Silicon Carbide Devices in High Efficiency DC-DC Power Converters for Telecommunications

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Abstract

The electrical efficiency of telecommunication power supplies is increasing to meet customer demands for lower total cost of ownership. Increased capital cost can now be justified if it enables sufficiently large energy savings, allowing the use of topologies and devices previously considered unnecessarily complex or expensive.

Silicon carbide Schottky diodes have already been incorporated into commercial power supplies as expensive, but energy saving components. This thesis pursues the next step of considering silicon carbide transistors for use in telecommunications power converters. A range of silicon carbide transistors was considered with a primary focus on recently developed, normally-off, junction field effect transistors.

Tests were devised and performed to uncover a number of previously unpublished characteristics of normally-off silicon carbide JFETs. Specifically, unique reverse conduction and associated gate current draw relationships were measured as well as the ability to block small reverse voltages when a negative gate-source voltage is applied. Reverse recovery-like characteristics were also measured and found to be superior to those of silicon MOSFETs. These characteristics significantly impact the steps that are required to maximize efficiency with normally-off SiC JFETs in circuits where synchronous rectification or bidirectional blocking is performed.

A gate drive circuit was proposed that combines a number of recommendations to achieve rapid and efficient switching of normally-off SiC JFETs. Specifically, a low transient output impedance was provided to achieve rapid turn-on and turn-off transitions as well as a high dc output impedance to limit the steady state drive current while sustaining the turned-on state. A prototype circuit was constructed using building blocks that are typically found in single chip MOSFET drivers. The circuit was shown to operate well from a single supply, alleviating the need for a split supply such as that required by many published JFET drive circuits. This demonstrated a proof of concept for a single chip JFET driver solution.

An active power factor correction circuit topology was extensively modelled and a prototype designed and tested to verify the model. The circuit was able to operate at

switching frequencies in excess of 100kHz when using SiC JFETs, whereas silicon MOSFETs could only achieve switching frequencies of several kHz before switching losses became excessive. The circuit was designed as the dc equivalent for a 2kW, 230V AC input power converter with a split +/-400V dc output.

A commercial single phase telecommunications power converter was modified to utilise normally-off SiC JFETs in its power factor correction circuit. The converter was tested and found to achieve similar electrical efficiency with 1200V SiC JFETs to that achieved with 600V silicon MOSFETs. The performance of the 1200V SiC JFETs in this application was also compared to that of 900V silicon MOSFETs and found to be superior.

Finally, a prototype three-phase cyclo-converter was modified to use 1200V normally-off SiC JFETs in place of 600V silicon MOSFETs and found to achieve similar electrical efficiency to the silicon MOSFETs in a 208V three phase system. These results strongly indicate that the 1200V SiC JFETs would provide better performance than 900V silicon MOSFETs in a 400V three phase system (that had been considered for commercial development).

Acknowledgements

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Publications associated with this thesis

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Contents

Chapter 1 Introduction

1.1 General

A broad range of silicon carbide (SiC) Schottky diodes is now commercially available following recent advances in SiC wafer production. These diodes have become popular in power factor correction circuits because their reverse recovery characteristics allow for significant improvements in switching losses to be achieved compared to silicon diodes [1-3].

Further research has brought about the development of a number of prototype SiC transistors including DMOSFETs [4], BJTs [5] and normally-off JFETs [6]. The high band-gap nature of SiC allows these transistors to block large voltages with a relatively small die [7]. A small die is advantageous for both cost of production and parasitic capacitance, creating the possibility that SiC transistors could offer unique benefits over status quo silicon transistors.

Telecommunication networks are transitioning from a highly centralized telephone exchange model to smaller, distributed nodes with an ever greater emphasis on data communications. A popular topology is “fibre to the node” where fibre optic cables carry high-speed communications data to equipment in a number of roadside cabinets (“nodes”) that convert the optical signals into electrical signals. These electrical signals are carried over the remaining distance to end customers via existing copper telephone cables [8]. The equipment in the roadside cabinets is typically powered by one or more small electronic power converters rated at 1-2kW. Recent advances in the design of these power converters have led to higher power conversion efficiency and reliability.

Recently, a very strong emphasis was placed on increasing the electrical efficiency of telecommunications power converters which has led to the adoption of more sophisticated materials and circuit topologies.

1.2 Scope and outline of thesis

This thesis focuses on the challenges and benefits of using the most recently developed SiC transistors for telecommunications power supplies. A large emphasis is placed on achieving high electrical efficiency as this is an important market driver. Steps involved in transitioning existing designs towards SiC transistors are explored in detail, whereas typical day-to-day product development activities common to any saleable power converter fall outside the scope of the thesis. Options considered mathematically are tested experimentally to ensure applicability of models to real world circuits and to ensure that parasitic elements and practical issues are adequately addressed.

The project was conducted in conjunction with an industry partner, providing essential insight and access to the latest telecommunications power supply technologies and trends as well as industrial resources. The industry partnership does pose some challenges to the scope of publication that is possible, because of commercial sensitivity. It also imposes constraints on some of the technical decisions made during the research to align it with commercial applications.

Chapter 2 provides an overview of typical telecommunications power converters, their market forces and explores potential applications where SiC transistors could offer competitive advantages. An overview of power factor correction circuits in telecommunications power supplies is given with a particular focus on the trend towards bridgeless topologies. The natural progression towards fewer series-conducting semiconductors is extended to the extreme case, leading to the topology studied in Chapter 6 through to Chapter 8. A specialized three-phase circuit analysis technique is described, which provides a language framework for the simple communication of the complex novel findings in Chapter 10. Three-phase single-stage power converters are discussed, contextualizing the topology tested in Chapter 10 with silicon carbide transistors.

0 evaluates several SiC transistor technologies that are becoming commercially viable including MOSFETs, BJTs and JFETs. Comparisons are drawn and predictions made for the conduction and switching losses of several transistors. The factors considered when choosing a transistor for further research are outlined and a decision made to pursue normally-off SiC JFETs. Finally, methods for driving normally-off SiC JFETs are

discussed including a timeline of developments in the literature that were published before and after the research in Chapter 5 was carried out.

In Chapter 4 a number of tests are conducted experimentally on a normally-off SiC JFET resulting in the identification of several unique characteristics. These novel characteristics have not been described previously in the literature. Knowledge of these characteristics is essential for achieving high efficiency in any application where substantial current is to flow through a SiC JFET in the source to drain direction, as for example in synchronous rectification. The characteristics have been presented by the author in [9] and [10].

In Chapter 5, a circuit is developed to achieve optimal driving of SiC JFETs. A prototype is built using components that are typically found in MOSFET driver integrated circuits to demonstrate the feasibility of a single-chip JFET driver. The circuit features a bipolar output and generates its own negative supply rail, allowing compatibility with single-ended auxiliary supplies.

Chapter 6 analyses a power factor correction (PFC) circuit topology that cannot be constructed with 600V silicon MOSFETs because of their inadequate voltage rating. The topology is also not viable at the desired switching frequency with 900V silicon MOSFETs because of their inadequate switching speed. Predictions are made for the performance of the topology with normally-off SiC JFETs.

The design of a prototype circuit for the DC equivalent of the PFC topology analysed in Chapter 6 is described in Chapter 7.

Testing methodologies and measured results for the prototype designed in Chapter 7 are presented in Chapter 8. Control issues in the implementation of the prototype circuit limit the maximum power level that can be attained. A good match is observed between the mathematical model in Chapter 6 and the measured performance at attainable power levels.

In Chapter 9, SiC JFETs are tested in a commercial telecommunications power converter and compared to silicon MOSFETs in this real world application. Newer SiC JFETs are also tested as well as a co-packaged parallel-connected pair of SiC JFETs.

Chapter 10 investigates the adoption of SiC JFETs into a three-phase cyclo-converter. A prototype converter is modified and operates successfully with SiC JFETs. Unique switching behaviour is observed, which has not previously been reported in the literature. The behaviour is caused by the JFETs' unique characteristics and can occur in a subset of the many three-phase power converter topologies. The effect is fully explained by mathematical analysis. The novel findings provide valuable insight into the adoption of SiC JFETs into a variety of three-phase topologies and have been presented by the author in [9]. Finally, the performance of the three-phase power converter prototype is compared with SiC JFETs and Si MOSFETs.

Chapter 11 summarizes the unique characteristics of the SiC JFETs investigated in this thesis and draws conclusions about the applications. The key findings from this research are discussed as well as the topologies most likely to benefit from the use of SiC JFETs. Finally a discussion is provided regarding future research work.

As part of the research in this thesis, investigations were conducted into the potential for a cascode connection to provide an effective means to drive SiC BJTs. Two cascode topologies were evaluated experimentally on silicon BJTs. Prohibitively high costs for engineering samples prevented the cascode circuits from being tested on SiC BJTs. Details of this research are included in Appendix A.

To supplement the schematic snippets discussed throughout this thesis, full schematic diagrams of all prototype circuits are provided in Appendix B. The manufacturer datasheets for the SJEP120R125 [11] and SJEP120R100 [12], two normally-off SiC JFETs studied extensively throughout the research are included for convenience in Appendix C and Appendix D. To assist the reader, references are made to Appendix C and Appendix D when referring to these datasheets.

Chapter 2 Background

This thesis is focused on the potential for deploying SiC transistors in telecommunications power supply applications. In this chapter, telecommunications power converter applications are discussed in detail, starting with market trends and application requirements. The use of active power factor correction (PFC) circuits in telecommunications power converters is discussed with a focus on recent trends toward bridgeless PFC topologies for improved efficiency. Trends in three-phase topologies are then described.

2.1 Telecommunications power converters

Telecommunications power converters are utilized across a broad range of telecommunication applications, most commonly to supply low voltage DC from an AC utility. In the telecommunications infrastructure market, these power converters are referred to as "rectifiers" because of their AC to DC rectification action. Line drivers in distributed roadside Digital Subscriber Line Access Multipliers (DSLAMs) for Plain Old Telephone Services (POTS) and Asynchronous Digital Subscriber Lines (ADSL) can draw up to 900mW per line with a single roadside DSLAM catering to as many as 900 customers [13]. Line drivers account for about 50% of a DSLAM's overall power consumption [13]. This has led to the popularity of 230V AC to 48V DC rectifiers with power levels in the 1.5-3kW range. Converters in this power range are produced by a number of manufacturers including Delta Energy Solutions [14], Eaton Powerware (Eaton) [15], Eltek Valere [16], Emerson Network Power [17] and SalTec Powerlink [18] who compete on price, electrical performance, reliability, form factor and other metrics.

2.1.1 Market trends

A number of factors have led to power electronics engineers focusing on the electrical efficiency of power converters. Data centre operators and telecommunications providers have begun to consider environmental and/or running costs when making purchasing decisions [19]. For a mobile communications network operator, energy consumption can make up 18%-33% of operating costs, depending on region and energy source [20]. This represents a significant portion of the total cost of ownership of a base station. A provider

may choose to pay a higher upfront price for higher efficiency equipment, if the added expense can be recouped through energy savings.

Some telecommunications providers have gone beyond simply comparing the total cost of ownership, when evaluating existing and potential equipment for their networks, to measuring useful performance. For example, in [21], performance is evaluated on the basis of a data rate throughput to power consumption ratio. By weighing up power consumption against useful performance during purchasing decisions, it can be ensured that reductions in power loss do not coincide with reductions in useful performance. There have also been investigations into the intelligent routing of telecommunication data based on energy consumption. By aggregating data over the most energy efficient equipment when multiple communications paths are available, less energy efficient equipment can be powered down during off-peak times [22].

In the context of power conversion, the push for higher conversion efficiency cannot cause detrimental reductions in output power or power quality attributes such as hold-up time, electromagnetic compatibility or noise. Achieving these goals requires a skilled design effort and the consideration of new technologies. Highly optimised control algorithms are often needed to achieve the desired levels of efficiency which has led to the development of dedicated integrated circuit controllers [23]. The LLC resonant converter topology has become particularly popular [24] due to its ability to achieve zero voltage switching (ZVS) on the primary side transistors and zero current switching (ZCS) on secondary-side synchronous rectifier devices [25]. The reduced emphasis on capital cost has also allowed the use of more expensive components such as Litz wire, trench MOSFETs and SiC Schottky diodes if their expense can be justified by energy savings.

Typical telecommunication rectifiers now achieve efficiencies in excess of 96% [14-16]. This represents a 50% reduction in losses compared to the approximately 92% efficient rectifiers [26-30] that were typically manufactured a few years ago.

2.1.2 Application requirements

One particular telecommunications power converter application is the 48V DC rectifier. Rectifiers draw a high power factor current waveform from a single phase utility and

deliver a low noise 48V DC output [31]. The output is used to supply equipment such as DSLAMs.

A number of countries are currently rolling out fibre to the node (FTTN) broadband networks to improve the internet data rates experienced by their customers such as Canada [32], Korea [33] and New Zealand [34]. In a FTTN network, fibre optic cables connect central switching offices to a number of DSLAMs, each of which connects to several hundred end users via copper wires. The standard typically used is the international telecommunications union G.922.5, colloquially referred to as ADSL2+. DSLAMs are often housed in roadside cabinets along with other switching equipment, all powered by one or more 48V DC rectifiers. The cabinets are often situated in residential areas, necessitating the minimisation of physical size and audible noise.

In addition to reducing running costs and environmental impact, higher electrical efficiency rectifiers assist with these physical size and audible noise constraints because their reduced power dissipation places less demands on thermal design. Specifically, smaller heat sinks and quieter, lower flow rate fans may be used.

Because telecommunications rectifiers operate from an AC utility source, they are subject to power quality regulations such as EN61000-3-2 and CISPR22. Compliance with such regulations fulfils the requirements set out in laws such as the European Commission's directive 2004/108/EC for electromagnetic compatibility and the United States Federal Communications Commission (FCC) requirements part 15. These regulations impose a number of constraints on the current waveforms drawn by rectifiers, particularly their harmonic content and power factors. This has further motivated the adoption of extensive input filters and active power factor correcting PFC boost converters in telecommunications rectifiers [35].

2.1.3 Potential for SiC transistors

With pressure from so many directions toward higher electrical efficiency, power electronics designers have already embraced new topologies and components to push the power conversion efficiency envelope. SiC transistors are viewed as components that could potentially allow for even higher electrical efficiencies to be achieved than currently possible with silicon devices. The active PFC circuits in telecommunications rectifiers are

particularly good candidates for SiC transistors because of their high switching speeds and blocking voltages, and are detailed more substantially in Section 2.2, and Chapter 6.

The high band-gap nature of SiC makes the characteristics of SiC transistors significantly different to those of their silicon counterparts. Specifically, the higher breakdown field strength of SiC compared to Si creates a shorter drift region, allowing a thinner die to be used to achieve a given blocking voltage [36]. After differences in the resistivity of the two materials is included, a larger ratio between blocking voltage and channel resistance has typically been observed in practical transistors [37]. This introduces the possibility for improving the conduction losses in a variety of hard-switched converter applications without compromising blocking ability. SiC transistors also require less semiconductor material to achieve a particular blocking voltage, leading to smaller parasitic capacitances. Parasitic capacitances have significant influence on the switching speed, particularly in series resonant converters [38]. With appropriate packaging, SiC transistors also have the potential for much higher operating temperatures in excess of 200°C [39]. Finally, smaller die sizes improve the long term economic feasibility of SiC transistors as the costs associated with SiC material decreases. A more detailed discussion of the different SiC transistors and their characteristics is provided in 0.

2.2 Single Phase Active Power Factor Correction

Regulations have imposed minimum power factor requirements on modern telecommunications equipment for example EN-61000-3-2 [40] which sets limits for the harmonic and power factor of electronic devices fused at less than 16A. This has led to power factor correction PFC circuits being designed into nearly all telecommunications power converters. Modern converters typically favour active PFC circuits over passive circuits because of the higher power factor that can be achieved without unreasonably large losses and magnetic component counts [41]. Because this thesis focuses on the applications of SiC transistors, the acronym PFC implies the active variety unless specified.

As manufacturers continue to compete on conversion efficiency, increasingly sophisticated PFC circuits have become commonplace to minimize circuit losses. It is already common as described in [1-3, 42] to use silicon carbide Schottky diodes to substantially reduce the losses that would otherwise have occurred due to the poor reverse recovery of many silicon

diodes. In [43], it was demonstrated that a significant proportion of the losses in many PFC topologies is contributed by the main power transistor(s). Transistors are therefore considered to represent a valuable opportunity for energy savings through the use of new transistor technologies.

A common trend in recent PFC circuits has been the introduction of bridgeless variants of common PFC topologies [44]. Bridgeless topologies typically shift some of the line frequency rectification process traditionally achieved by a full diode bridge to one or more semiconductors that are also responsible for forming part of a power converter. This is generally done in such a way as to reduce the number of series conducting diodes and transistors such that higher conversion efficiency is achieved via reduced conduction losses.

2.2.1 Boost converter based PFC topologies

The classic PFC topology, shown in Figure 2-1 consists of a diode bridge rectifier, formed by D2-D5 feeding a boost converter consisting of L1, D1, Q1 and C1. By using a boost converter to boost the rectified sinusoidal input to a DC output where the voltage is larger than the peak of the input sinusoid, a power factor close to unity can be achieved by varying the duty cycle of a PWM signal applied to Vg [45].

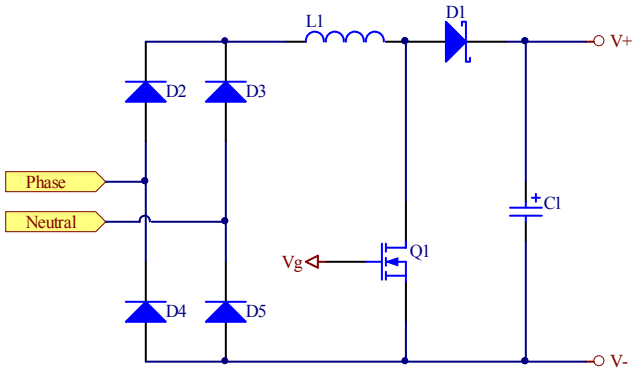


Figure 2-1: Classic active power factor correction topology

The quest for higher conversion efficiency has led to many power converter designers abandoning the classic topology in favour of more sophisticated alternatives [46]. One of the simplest alternatives to the classic PFC circuit is the bridgeless version shown in Figure 2-2 [47, 48], where L1, D1 and Q1 form a standard boost converter while L2, D2 and Q2

form a second boost converter in parallel. During positive mains half-cycles, Q2 is kept on while Q1 is driven with PWM. Current always flows through two semiconductors, either Q1 and Q2 or D1 and Q2. During negative half-cycles, Q1 is held on while Q2 is driven with PWM and current flows alternately through Q1 and Q2 or Q2 and D1. This is an improvement over the classic topology in Figure 2-1 where current always flows through three semiconductors, two of the bridge diodes and either D1 or Q1.

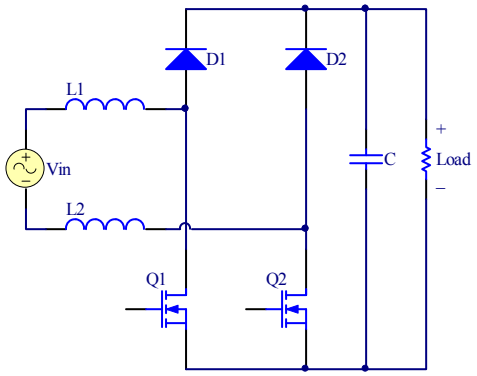


Figure 2-2: Simple bridgeless PFC circuit

Unfortunately the topology in Figure 2-2 exhibits significant common mode noise because the output is not tied to either of the mains input terminals [49]. In [50], two bypass diodes were added to improve the EMI as shown in Figure 2-3, and recently [51] discussed the use of a common addition of two bypass diodes to improve the common mode noise, though this results in poor utilization of magnetic components as each inductor is only used half of the time.

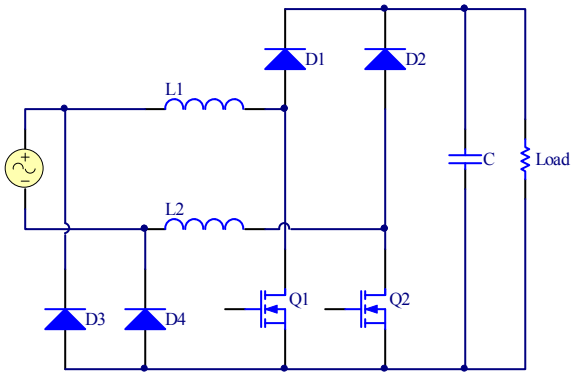


Figure 2-3: Bridgeless PFC circuit with bypass diodes

In [44], it was shown that the topology in Figure 2-3 can be rearranged as shown in Figure 2-4 where Q1 and Q2 form a bidirectional switch and only one inductor is needed.

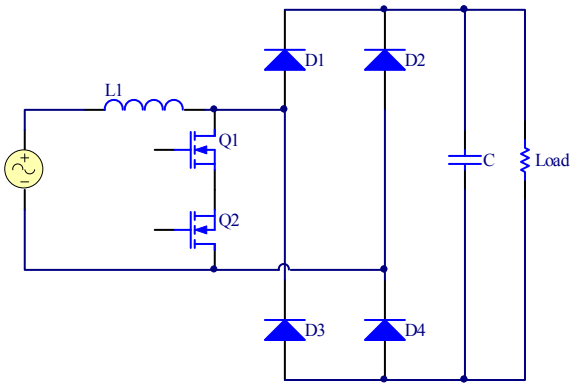


Figure 2-4: Bridgeless PFC circuit with bidirectional switch

In [52], the topology in Figure 2-2 was extended to use two paralleled converters operating 180° out of phase as shown in Figure 2-5. This 'interleaving' mode of operation reduces the current ripple at the input, aiding EMI filter design. The topology also achieves a reduction in conduction losses compared to Figure 2-2 because of the doubled up inductors and transistors, though switching losses are likely to be increased.

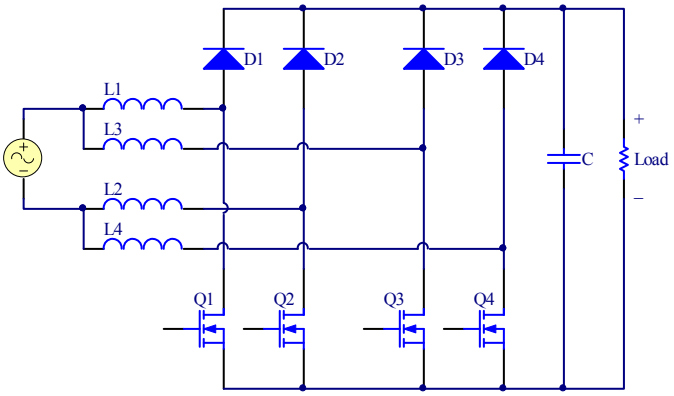


Figure 2-5: Bridgeless interleaved PFC circuit

Extending the minimization of series-conducting semiconductors further leads to the well known half-bridge topology shown in Figure 2-6 [48]. In this topology only one semiconductor conducts at any time.

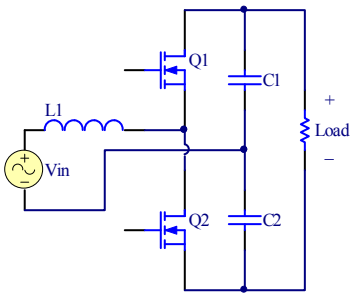


Figure 2-6: Half bridge PFC circuit

The main drawback of the half-bridge PFC circuit in Figure 2-6 is that the transistors must block twice the voltage of those in any of the other topologies discussed in 2.2.1. For an input voltage of 230V RMS, as is common in much of Australasia and Europe, the peak voltage of 325V dictates that the output voltage be at least 650V. This precludes the use of the latest 600V MOSFETs which could be used in other topologies. Conventionally, higher voltage MOSFETs or IGBTs would need to be used instead which exhibit much poorer switching speeds.

2.2.2 Buck-boost based PFC topologies

The trend towards bridgeless PFC circuits has also been observed with buck-boost based designs. Figure 2-7 shows an PFC circuit based on the Single Ended Primary Inductor Converter (SEPIC), a member of the buck-boost family [53].

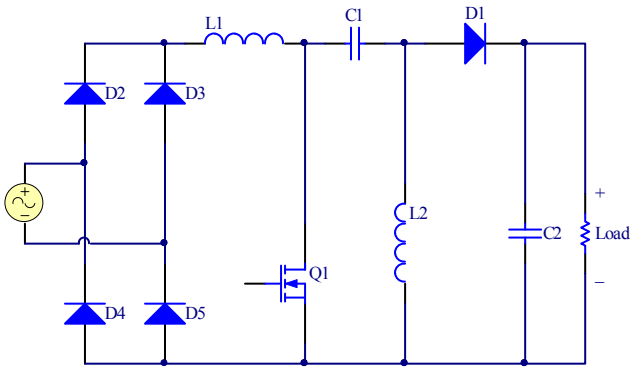


Figure 2-7: SEPIC based PFC

A bridgeless version of the SEPIC PFC, shown in Figure 2-8 was proposed in [54]. The bridgeless SEPIC PFC has only two series conducting semiconductor devices at any time compared to three in the classic SEPIC PFC from Figure 2-7, resulting in improved conduction losses.

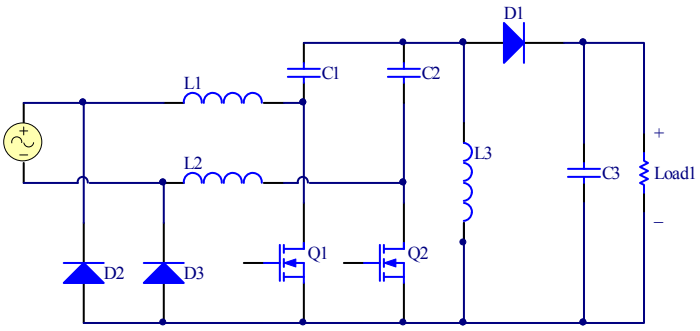


Figure 2-8: Bridgeless SEPIC based PFC topology

If the positions of D1 and L2 in the SEPIC based PFC from Figure 2-7 are swapped and the output polarity reversed, the closely related Ćuk based PFC circuit in Figure 2-9 is created.

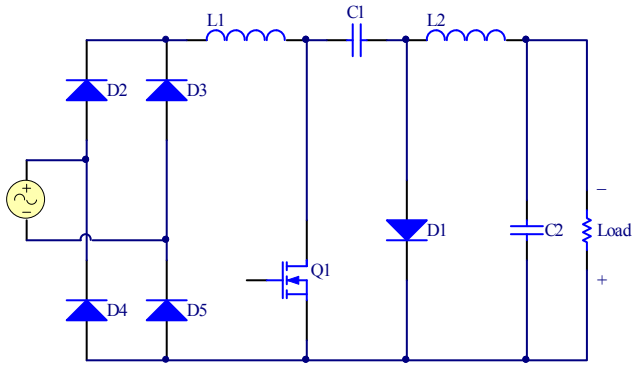


Figure 2-9: Ćuk based PFC

A bridgeless variant of the Ćuk based PFC shown in Figure 2-10 was proposed in [54] to reduce the number of series conducting semiconductor devices from three to two. This allows a significant improvement in conduction losses to be achieved.

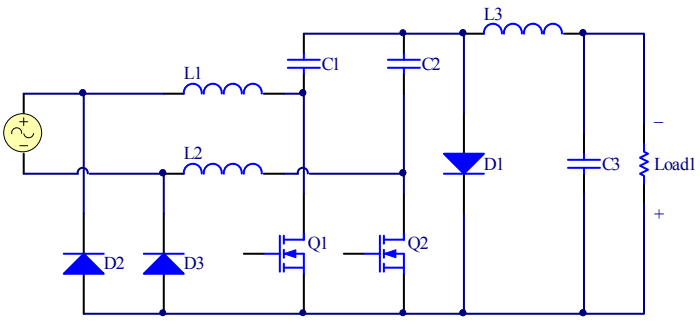


Figure 2-10: Bridgeless-Ćuk based PFC

2.2.3 Single Phase PFC Toplogy for SiC Transistors

The single phase boost converter topology in Figure 2-6 is the single phase PFC topology expected to be the most likely to benefit from the use of SiC transistors as it is able to more of their blocking voltage capabilities than other topologies. Meanwhile, the reduced number of series conducting semiconductors has the potential to achieve excellent conversion efficiency through reduced conduction losses.

2.3 Specialized three-phase terminology

Typically, the three physical connections to mains utility phases are referred to statically using labels such as A, B, C; 1, 2, 3; or red, yellow, blue to refer to the three physical connections. If the three phases coming into a converter are instead assigned dynamic labels based on their instantaneous absolute voltages, analysis becomes much easier. For example, if the phase exhibiting the largest absolute voltage magnitude at any point in time is referred to as "large" and the phase exhibiting the smallest absolute voltage as "small". The remaining phase is then referred to as "medium", resulting in a useful analysis and communication framework. Figure 2-11 shows one cycle of normalized three-phase mains voltages against time, divided into twelve segments with the labels 'L', 'M', 'S' applied dynamically to the large, medium and small phases respectively in each segment.

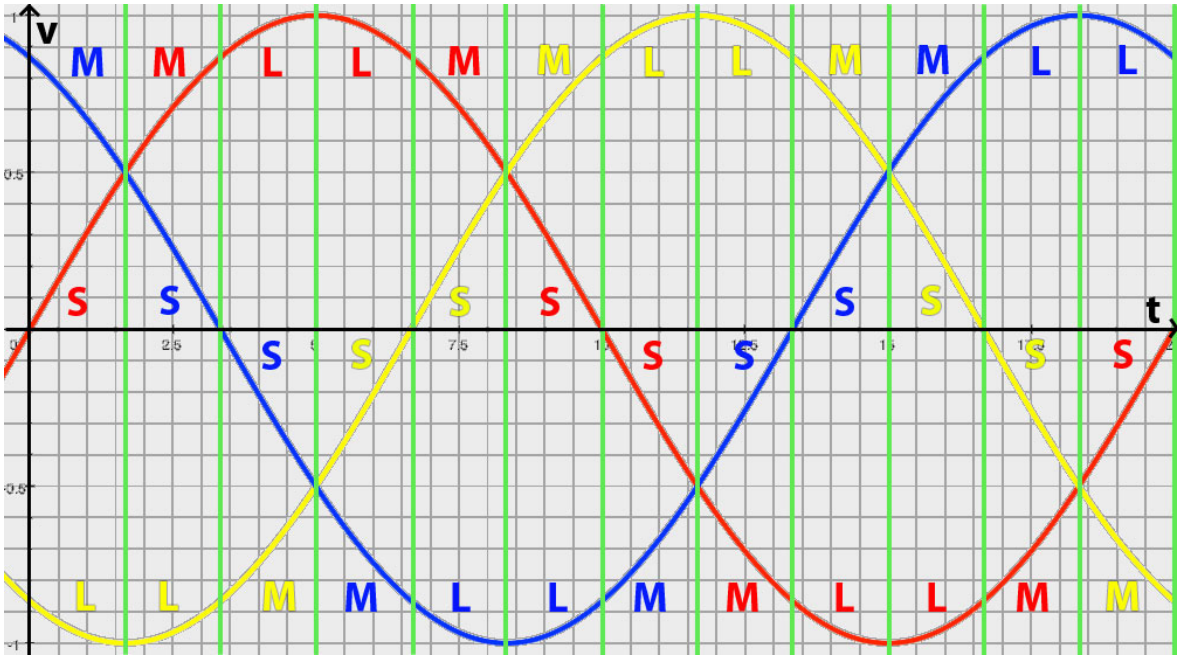


Figure 2-11: Large, medium, small classification for three-phase terminology

The framework is useful because a single 20ms mains cycle may be divided into three equally spaced segments that are symmetrically identical to one another if the large/medium/small labelling is applied. Each of these generic segments can then further be divided into four sub-segments that are mirror images of one another through reflection in time and polarity. The corollary is that just one twelfth of a mains cycle is representative of an entire mains cycle, through symmetry. This paradigm is a valuable tool when abstracting or communicating complicated switching sequences in three-phase power converters. The notation will be used in the following sections of this Chapter and throughout Chapter 10.

2.4 Three-phase AC to DC power converters

Significant advances have been made over the years in three-phase AC to DC power converter technology. Of particular interest for achieving high efficiency are a family of power converters that directly convert three-phase AC to single-phase, high frequency AC in a single stage. This allows connection of a high-frequency transformer without the traditional need for a separate rectifier, DC link and inverter. The combination into a single stage is similar to the trend of using bridgeless topologies in single-phase PFC circuits and similarly achieves reductions in the number of series conducting semiconductor switches and, consequently, conduction losses.

2.4.1 Six primary-side bidirectional switch topology

In [55], a three-phase AC to DC power converter was proposed using the topology shown in Figure 2-12.

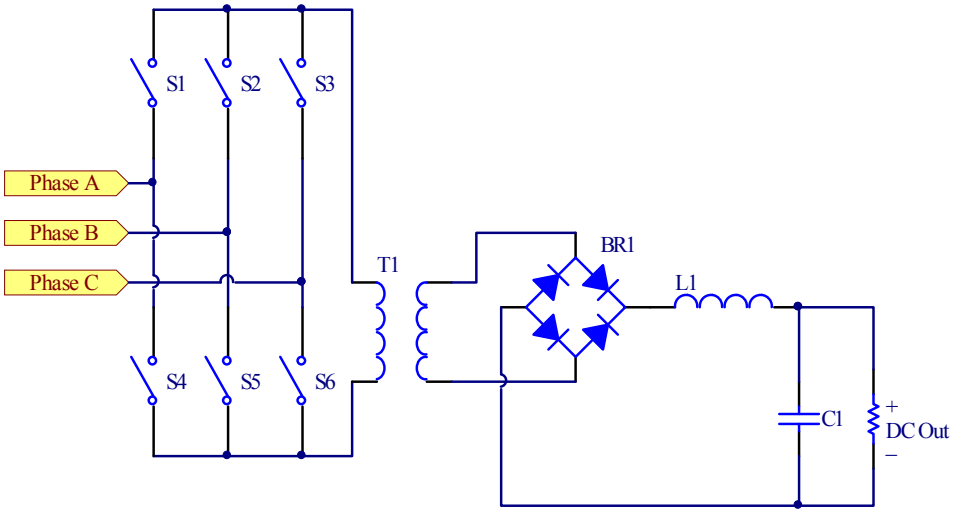


Figure 2-12: Three-phase AC to DC power converter topology

A high frequency AC signal was created at the primary of transformer T1 by turning on different combinations of switches in sequence. At any particular time, only one upper and one lower switch were turned on. Sinusoidal PWM was performed on the switches to ensure that all three AC input currents were sinusoidal and in phase with their respective voltages to achieve unity power factor and low distortion. Fast rectifier diodes were used in BR1 to rectify the high frequency output at the secondary of T1. The primary side bidirectional switches in [55] were realised using the circuit shown in Figure 2-13.

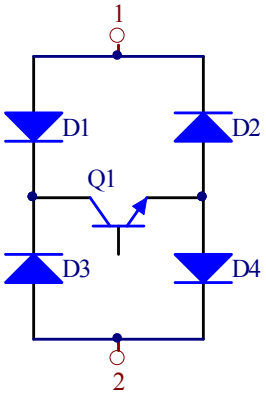


Figure 2-13: Bidirectional switch realisation in [55].

Each turned-on bidirectional switch represented three series conducting semiconductor devices, with a total of six series conducting primary side semiconductors at any time. Following a similar trend to that observed in single-phase PFC topologies, the number of series conducting semiconductors at any time was reduced from six to four in [56] by realising the bidirectional switches with pairs of back-to-back MOSFETs. The MOSFETs'

parasitic output capacitances and the transformer's leakage inductance, represented by L1 in Figure 2-14 were utilized to achieve zero voltage transitions.

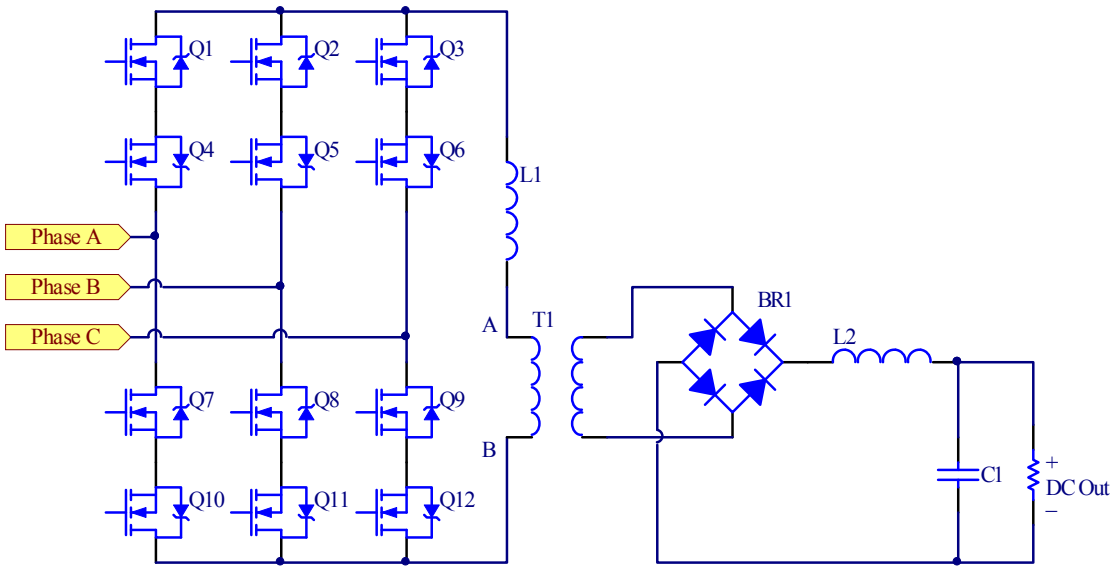


Figure 2-14: Three-phase AC to DC power converter with back-to-back MOSFET switches

A special switching pattern was used to drive the appropriate combinations of transistors to result in a sequence of different combinations of two AC phases being connected across the primary of T1. Each new combination in the sequence was immediately followed by the same combination again, but with opposite polarity and then a dead time. By adjusting the ratio of time with two phases connected to T1 and dead time, PWM control was achieved, allowing the DC output to be regulated by a control loop. It is important to note that the pairs of transistors in each bidirectional switch were not always switched in unison. This allowed bidirectional switches to be configured in a one-way conducting state to assist with turn-on transitions and provide a path for freewheeling current during dead times. Using the specialized three-phase terminology described in section 2.3, the simplified general switching sequence, ignoring the one-way conducting transition states is summarized in Table 2-1.

Combination	T1 terminal A connected to	T1 terminal B connected to
1	Large phase	Medium phase
2	Medium phase	Large phase
Dead time	-	-
3	Large phase	Small phase
4	Small phase	Large phase
Dead time	-	-

Table 2-1: Switching pattern of three-phase power converter

In [57], a 2kW prototype converter was constructed and operated from a 208V RMS phase to phase input voltage. The output was set at 50V DC and a switching frequency of 91kHz was used. An efficiency of approximately 93% was achieved.

2.4.2 Three primary-side bidirectional switch topology

In [58, 59], half of the bidirectional switches from the topology in 2.4.1 were replaced with capacitors as shown in Figure 2-15. This reduces the number of series conducting primary side switches from two to one, improving conduction loses.

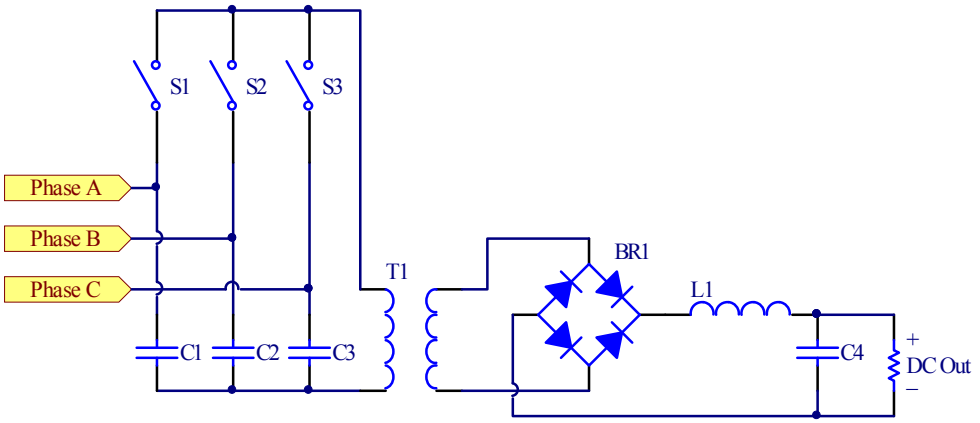


Figure 2-15: Thee primary-side switch, three-phase AC to DC topology

The remaining three bidirectional switches were realised using back to back pairs of MOSFETs instead of the three series conducting semiconductor scheme in Figure 2-13. This results in an overall realization of just two primary side series-conducting semiconductor devices at any time compared to the six in Figure 2-14, allowing a very significant improvement in conduction losses to be achieved. Figure 2-16 shows the full

realization of the three primary-side bidirectional-switch topology for three-phase to DC conversion.

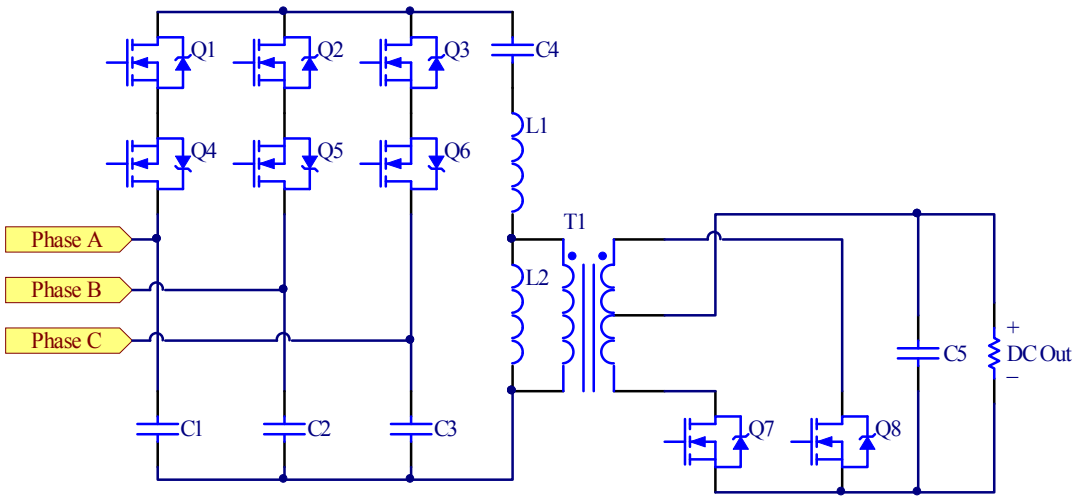


Figure 2-16: Three bidirectional switch, three phase cyclo-converter

C4 and L1 form a series resonance, allowing power flow from the primary to secondary to be controlled by varying the fundamental frequency of the current through T1's primary. Switching the phases in the pattern large, medium, small and leaving the appropriate transistors turned on to achieve clamping through body diodes, most transitions are able to be conducted under zero-voltage conditions, minimizing switching losses.

The use of Q7 and Q8 to achieve synchronous rectification on the DC side provides another reduction in conduction losses compared to those exhibited by the topology in Figure 2-14, as does the removal of the output inductor on the DC side. This poses problems for regulating the output voltage at light loads which are mitigated by the addition of inductor L2. A conversion efficiency of 97% can be achieved with this topology [59].

The proprietary switching patterns described in [59] cause current to generally flow in one direction through the large phase and return in the opposite direction through both the medium and small phases. By carefully adjusting the ratio of current through the medium and small phases, unity power factor can be achieved. Variations are made to the switching pattern around zero crossings and the points where the magnitudes of medium and small phases cross (magnitude crossings) whose exact points in time are impractical to measure

with sufficient accuracy to maintain the normal switching sequence. Near zero crossings, the small phase's switches remain off and a large-medium pattern is followed. Near magnitude crossings, a pattern of large, medium, large, small is repeated. The testing of a prototype rectifier based on [59], retrofitted with silicon carbide transistors is described in Chapter 10.

2.4.3 Three-phase SEPIC rectifier with reduced transistors

During the time period between the development of the topologies in 2.4.1 and 2.4.2, a new three-phase rectifier topology shown in Figure 2-17 was proposed in [60].

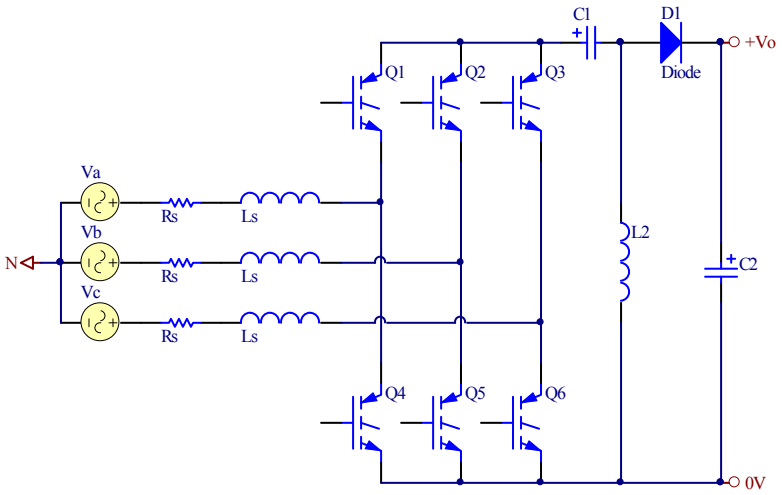


Figure 2-17: SEPIC topology with reduced number of series-conducting semiconductors

The topology in Figure 2-17 is based on the SEPIC Vienna rectifier topology proposed in [61] and shown in Figure 2-18. The topology in Figure 2-17 requires twice as many transistors as the topology in Figure 2-18, but features a reduced number of series-conducting semiconductors at any time, to reduce conduction losses.

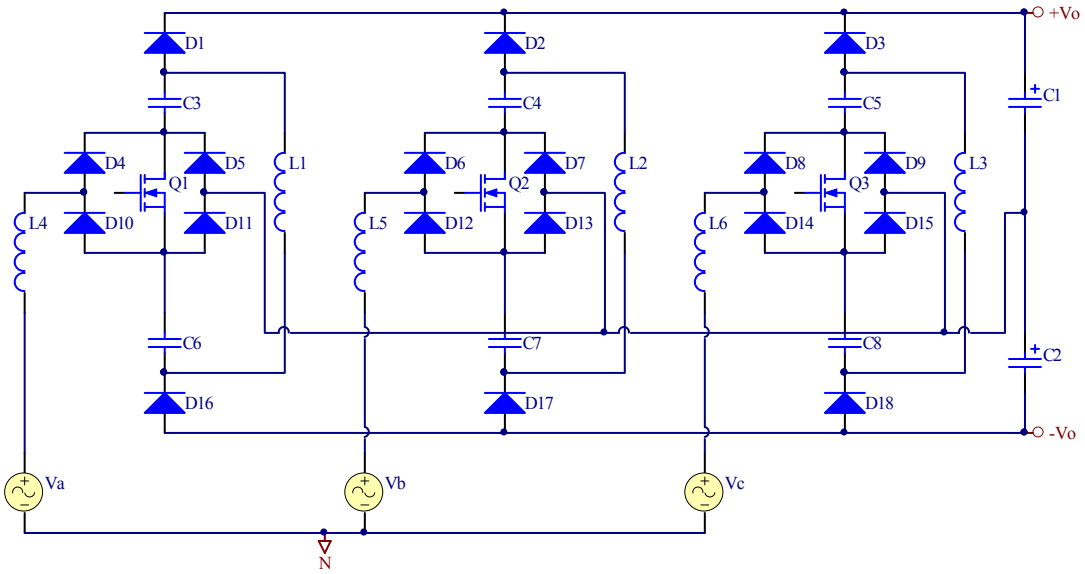


Figure 2-18: Three-phase SEPIC topology [61]

2.5 Conclusion

A number of bridgeless single phase power factor correction circuits from the literature have been discussed as examples of achieving improved conduction losses through reductions in the number of series conducting semiconductors. Without counting paralleled semiconductors as less than one, it appears that the minimum number of series conducting semiconductor switches for a single phase active PFC circuit is one. Figure 2-6 is an example of a topology featuring only one series conducting semiconductor at any time, with the trade-off being the requirement of transistors possessing twice the blocking voltage of that needed by many other topologies. This topology forms the basis of the PFC application designed, constructed and tested with SiC transistors in Chapter 6 through to Chapter 8 to evaluate whether high voltage SiC transistors can offer better performance in this topology than what can be achieved with silicon transistors.

A reduction in series conducting semiconductors in the literature was also discussed for three-phase rectifiers. The patented topology in Figure 2-16 achieves isolated three-phase AC to DC conversion with just two series conducting primary-side semiconductors. This allows excellent efficiency to be achieved and a 208V line to line rectifier for the low voltage United States markets can be constructed using this topology with 600V silicon MOSFETs. For the 415V line to line three-phase systems in Europe or the 480V line to line industrial connections in the United States, higher voltage transistors are required. High voltage SiC transistors could offer better performance than silicon transistors in these

high voltage variants. This topology is therefore used as a platform for testing SiC transistors in a three-phase PFC application in Chapter 10.

Chapter 3 SiC Transistors

Several SiC transistors have reached or are nearing sample availability. They cover a broad range of transistor types and are developed by a small number of different manufacturers. In this chapter, a range of SiC transistors are considered and compared. The normally-off SiC JFET is chosen for further research activities and the reasons for the decision are discussed. Finally, the gate drive requirements of the normally-off SiC JFET are investigated.

3.1 SiC MESFETS

The United States National Aeronautics and Space Administration (NASA) has a research programme to develop new SiC semiconductors for harsh aerospace environments. Prototype devices have demonstrated operation of logic gates based on SiC MEtal Semiconductor Field Effect Transistors (MESFETs) operating at 600ºC [62]. An amplifier consisting of a transistor, ceramic capacitor and two resistors has also been demonstrated to exhibit stable operation for 430 hours at 500ºC. The MESFETs were fabricated using SiC wafers from Cree Inc (Cree) [63].

Over the time period covered by the research in this thesis, many advances have been made in SiC MESFET technology, however devices being produced at the conclusion of the research were very much tailored to RF applications with amplifiers in the gigahertz range demonstrated [64-66], however the voltage ratings of these devices were in the tens of volts and therefore not suitable for power conversion applications.

3.2 SiC MOSFETS

MOSFETs are being investigated in the literature as a major area of research, with preliminary information available from Cree for prototype devices. Historical gate oxide reliability issues have undergone significant improvements recently [67] to the point that there is now little reason for concern [68]. Mitsubishi Electric claims to have developed a

SiC MOSFET based inverter for driving 3.7kW motors with 50% less power loss than existing motor drives [69].

SiC MOSFETs have a lower transconductance than silicon MOSFETs, though their threshold voltage is similar. These characteristics make SiC MOSFETs sensitive to unintentional turn-on and a negative gate bias is sometimes required to ensure reliable turn-off [70]. The SiC MOSFET does not exhibit a flat Miller plateau and exhibits a subtle transition between its ohmic to saturation regions. Because of this, it is recommended that gate drive voltages as high as 20V are used [70].

At the time of selecting SiC transistors for use in this research, Cree had an unpublished preliminary data sheet for a SiC power DMOSFET [71]. The device is a N-channel enhancement mode MOSFET capable of carrying 20A and blocking 1200V. The typical on resistance for this MOSFET is 107mΩ at 25°C, V_{GS}=15V.

Switching performance data is provided for an inductive load drawing 10A from a 600V supply. At 25°C, the MOSFET turn-off energy is approximately 125μJ, increasing to 155μJ at 150°C.

Around the time of completing the research in this thesis an updated datasheet was available for the Cree CMF1020D 24A SiC MOSFET with a rated channel resistance of 160mΩ [72]. A new a 42A 1200V SiC MOSFET had also been announced with an on resistance of 80mΩ [73].

3.3 SiC BJTs

SiC BJTs are being manufactured in small quantities and promise incredibly rapid switching speeds. This makes SiC BJT development a promising technology, although concerns have been expressed that SiC BJTs can experience current gain degradation after periods of stress [74].

Transic Corp (Transic) is a key manufacturer of SiC BJTs. The company has developed two prototype SiC BJTs: the BitSiC1206 and the BitSiC0620. The BitSiC1206 is rated to carry 6A and to block 1200V whilst the BitSiC0620 is rated at 20A and 600V. The BitSiC1206 is closer to commercial availability and offers the same 1200V blocking

voltage as the Cree MOSFET. The BitSiC1206 is available in bare die form as well as in several packages such as TO-247 and in a high temperature metallic case. The BitSiC1206 has a saturation voltage between 1.4V and 1.5V at full load of 6A, suggesting a conduction loss of 9W [75].

A waveform is available for the BitSiC1206 when switching a 6A inductive load at 500V [76]. The turn-off time is listed as 40ns but the temperature is not specified. Piecewise linear approximations of the waveform indicate a turn-off energy of approximately 60μJ.

Several examples of applications using SiC BJTs have been seen in the literature. In [77], a 300W PFC circuit was constructed with SiC BJTs and achieved switching frequencies of 400kHz at a junction temperature of 150°C. A drive circuit for SiC BJTs was demonstrated in a 280W inverter in [78], with simulations predicting an efficiency of 96-97% for a 2kW inverter.

Around the time of completing the research in this thesis, TranSiC were acquired by Fairchild Semiconductor Corporation (Fairchild) [79], suggesting that their SiC BJT technology is likely to be further developed and commercialized in the future.

3.4 Normally-on SiC JFETs

Several manufacturers, most notably SiCED GmbH, have developed prototype SiC junction field effect transistors. SiC JFETs typically exhibit 'normally-on' characteristics, requiring a negative gate bias of several volts in order to realise their full rated blocking voltage. This can cause problems in typical power converter designs which rely on transistors blocking during start-up. It affects reliability because transistor driver failure with normally-on transistors creates a short-circuit condition in many bridge and boost topologies.

With the reliability and failure-mode issues associated with normally-on transistors, many techniques have been developed to protect against catastrophic failure should a gate drive circuit fail. There are many examples of high voltage normally-on SiC JFETs being connected in cascode with a low voltage silicon MOSFET [80-86]. It is also possible to create a low voltage normally-off SiC JFET suitable for use in cascode with high voltage

normally-on SiC JFETs [87] to achieve a normally-off compound switch. The popularity of the cascode connection of normally-on SiC JFETs has led to the development of a normally-on JFET that is co-packaged with a silicon MOSFET [87].

Although the cascode connection solves many of the problems caused by the normally-on characteristic, the additional complexity of many of these solutions still makes the use of SiC JFETs unattractive. In addition, the cascode must necessarily allow the full load current of the high voltage normally-on SiC JFET to flow through the low voltage transistor, resulting in increased conduction losses. The increase may however be negligible. During the period of the research, [81] proposed a Si MOSFET/SiC JFET cascode combination where the channel resistances of the SiC JFET and Si MOSFET were 65mΩ and 2mΩ respectively, representing only a 3% increase relative to the JFETs own conduction losses. Circuits for driving normally-on SiC JFETs directly have also been proposed [88, 89]. These circuits avoid the conduction loss penalty of the cascode Si MOSFET as well as its thermal limitations.

New normally-on SiC JFETs were also announced during the period of the research [90], [91]. For the purposes of comparison in 3.6-3.8, the SJDP120R085 normally-on SiC JFET from SemiSouth will be used. The SJDP120R085 is a 1200V 27A device with a channel resistance of 85mΩ and a maximum operating temperature of 150°C.

When evaluating the potential of using normally-on SiC JFETs in PFC circuits for telecommunications rectifiers, it should be noted that a 100W prototype was demonstrated in [92] with an efficiency of 95.5%.

Normally-on SiC JFETs continue to be an active field of research with many innovations published over the period of the research in this thesis. In [93], a 99% efficient 3.5kW inverter was demonstrated using normally-on SiC JFETs. In [94], a balancing technique was devised, allowing 6 normally-on SiC JFETs to be connected in series to create a higher voltage switch. This in turn was used to construct a 5kV pulse generator with 50ns transitions. Meanwhile, [95] demonstrated a high temperature packaging for multiple paralleled normally-on JFETs, forming the output stage of a 50kW inverter for operation at 200°C. Toward the end of the research presented in this thesis, SiCED was acquired by

Infineon Technologies (Infineon), suggesting that further development and commercialization of their normally-on SiC JFET technology is likely.

3.5 Normally-off JFETs

SemiSouth Inc (SemiSouth) has developed a SiC JFET with significantly different characteristics to other SiC JFETs. The SemiSouth SJEP120R125, characterised extensively in the following chapter, exhibits a normally-off characteristic, blocking 1200V without any gate bias or cascode connection. The SJEP120R125 has a current rating of 15A continuous at 125°C.

Turn-off energy data is available [Appendix C] at 600V over a range of loads up to 15A. Data is provided for temperatures of 25°C and 150° with insignificant variation between the two. At 6A and 10A, the turn-off energy is approximately 35µJ and 75µJ respectively with a gate resistance of 5Ω and the turn-on energy for 6A and 10A is 45µJ and 70µJ respectively. The normally-off JFET has a maximum junction operating temperature of 175°C [Appendix C].

Prior to the research in this thesis, an inverter using normally-off SiC JFETs was demonstrated in [96]. Synchronous rectification was also demonstrated, but efficiency was left as future work. In [97], 600V 2A normally-off SiC JFETs were used to construct an inverter that drove a 50W fan with an efficiency of 96.4%.

During the time covered by the research in this thesis, further advances were made with normally-off SiC JFETs. In [98], a normally-off SiC JFET was tested as a drop-in replacement for an IGBT in a PFC circuit, achieving an efficiency improvement of nearly 1%. Similar results were demonstrated in [99] where normally-off SiC JFETs were tested as drop-in replacements for IGBTs in a commercial solar string inverter. Here too, an efficiency improvement of nearly 1% was achieved. In [100], a photovoltaic inverter was designed with normally-off SiC JFETs and demonstrated to achieve a peak efficiency of 98.8%.

In the literature and this thesis, normally-off JFETs are also referred to as enhancement mode (EM) JFETs. Around the time that this thesis was completed, SemiSouth went out of business [101].

3.6 Basic comparison of switching performance

Based on the information supplied by manufacturers during the time of the research [71], [76], [Appendix C], [75], [90] the turn-off energy of several SiC transistors is tabulated in Table 3-1. Whilst the test scenarios for these devices are not identical, a rough measure of the relative turn-off performance is achieved. None of the manufacturer datasheets used for the information in Table 3-1 stated the measurement error, so the values are considered to be approximate.

Device	Voltage	Current	Rated Current	Turn-off energy	Gate resistance	Temperature
Cree MOSFET	600V	10A	20A	155µJ	20Ω turn-on, 4Ω turn-off	150°C
Transic BJT	500V	6A	6A	60µJ	300mA base current	100°C
SemiSouth EM JFET	600V	10A	15A	75µJ	5Ω	150°C
SemiSouth EM JFET	600V	6A	15A	35µJ	5Ω	150°C
SemiSouth normally-on JFET	600V	10A	27A	60µJ	5Ω	150°C

Table 3-1: Comparison of turn-off energy based on manufacturer supplied data for inductive loads

Under equal voltage, current and temperature conditions, the SemiSouth EM JFET exhibits lower turn-off energy (75µJ) than the Cree MOSFET (155µJ). For voltage and temperature conditions that favour the Transic BJT, the SemiSouth EM JFET has a lower turn-off energy (35µJ) than the Transic BJT (60µJ). The SemiSouth normally-on JFET has slightly lower turn-off energy than the EM JFET under equal voltage, current and temperature conditions.

Turn-on energy was similarly extracted from the available datasheets and literature, and is presented in Table 3-2.

Device	Voltage	Current	Rated Current	Turn-on energy	Gate resistance	Temperature
Cree MOSFET	600V	10A	20A	120µJ	20Ω turn-on, 4Ω turn-off	150°C
Transic BJT	500V	6A	6A	60µJ	300mA base current	100°C
SemiSouth EM JFET	600V	10A	15A	70µJ	5Ω	150°C
SemiSouth EM JFET	600V	6A	15A	45µJ	5Ω	150°C
SemiSouth normally-on JFET	600V	10A	27A	105µJ	5Ω	150°C

Table 3-2: Comparison of turn-on energy based on manufacturer supplied data for inductive loads

As with turn-off energy, the Cree MOSFET has the worst turn-on energy at 600V, 10A 150°C. For turn-on, SemiSouth's normally-on JFET fares worse than their EM JFET. The Transic BJT exhibits higher turn-on energy than the EM JFET despite more favourable temperature and voltage conditions.

For a single phase converter at a nominal 230V RMS, a sinusoidal input current with a peak of 6A would provide 976W. It is therefore viewed that although the TranSiC BJT has potential for small power converter applications, it does not have sufficient current carrying capacity for use in 1.5-2kW telecommunications power converters without paralleling several devices.

Table 3-3 summarizes the turn-on and turn-off losses of the JFETs and MOSFET at 10A, 600V, 150°C. This gives a relative indication of the switching losses that could occur in a hard-switched power converter.

Device	Turn-off energy	Turn-on energy	Total energy
Cree MOSFET	155µJ	120µJ	275µJ
SemiSouth EM JFET	75µJ	70µJ	145µJ
SemiSouth normally-on JFET	60µJ	105µJ	165µJ

Table 3-3: Turn-on and turn-off energy at 600V, 10A, 150°C.

The EM JFET exhibits the lowest switching energy for a hard-switched 600V, 10A inductive load at 150°C with the normally-on JFET a close runner up. The Cree MOSFET would exhibit significantly higher losses than either JFET in a hard-switched application, limiting its appeal in hard-switched converters. In converters with zero-voltage turn-on, the turn-off energy of the Cree MOSFET still makes it a poor choice compared to the SemiSouth JFETs.

3.7 Basic comparison of conduction losses

In addition to the switching characteristics of a power converter, conduction losses are an important factor. Manufacturer supplied data were used to calculate the voltage drop of each transistor up to its maximum continuous current rating. This allowed the conduction losses (for continuous conduction) to be calculated.

Characteristic curves are available for the SJEP120R125 EM JFET [Appendix C], SJDP120R085 normally-on JFET [90], BitSiC1206 BJT [75] and Cree MOSFET [71]. The SJEP120R125 was modelled for a gate-source voltage of 3V and the Cree MOSFET at a gate-source voltage of 20V. The conduction losses for these devices are shown in Figure 3-1.

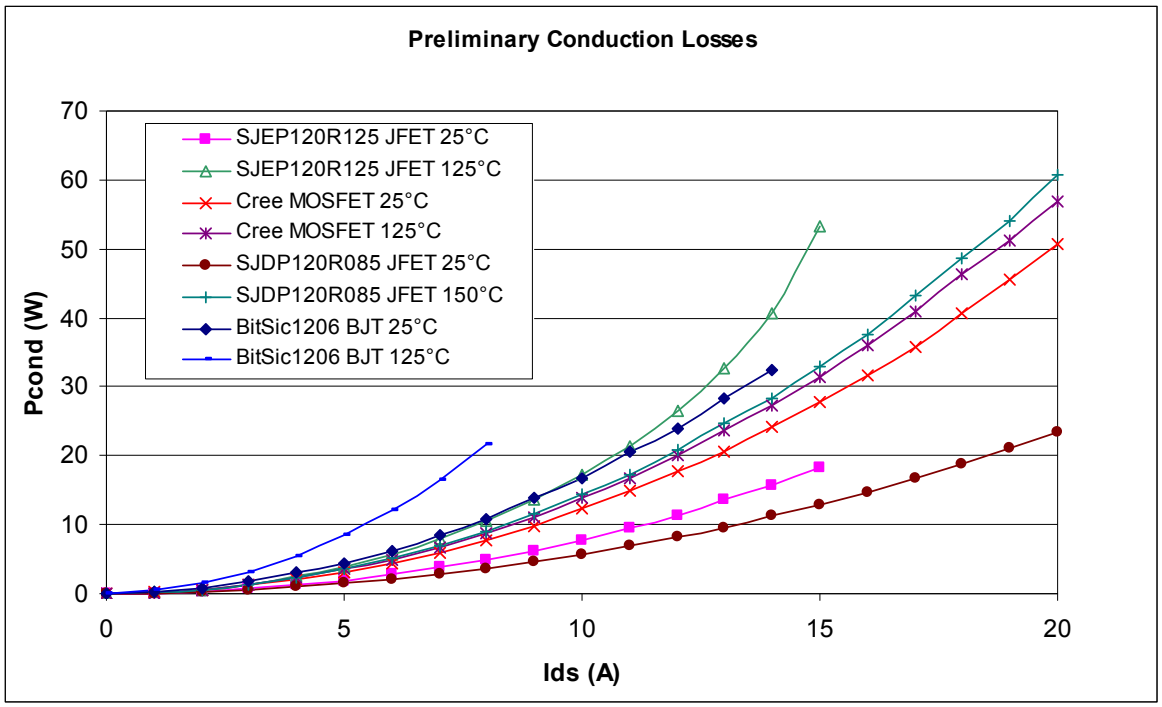


Figure 3-1: Conduction losses based on manufacturer data for different SiC transistors

The SJDP120R085 normally-on JFET and SJEP120R125 EM JFET offer the lowest conduction losses at 25°C, better than the Cree MOSFET; however, the losses of these devices are highly temperature dependent and deteriorate more than those of the Cree MOSFET, resulting in poorer performance than the MOSFET at elevated temperatures. It is important to consider that 25°C is not a typical operating point for a transistor that is dissipating tens of watts. At the same time, temperatures in excess of 125°C are likely to leave little thermal margin and are therefore more of a worst case than a typical operating condition. The typical operating temperatures of the transistors are likely to be somewhere in between for most applications. The conduction losses of the MOSFET and JFETs are therefore likely to be fairly similar in many applications.

Regardless of operating temperature, the normally-on JFET is going to exhibit lower conduction losses than the EM SiC JFET. This is expected since it has a 32% lower nameplate channel resistance. The TranSiC BJT meanwhile is the worst performer, with higher conduction losses than any other transistor at similar temperatures.

3.8 Comparison of rated junction temperatures

Based on the information available early on in the research, the maximum operating temperatures and junction-case thermal impedances of several SiC transistors packaged in TO-247 cases were compared, with their characteristics listed in Table 3-4. A thermal impedance figure for a packaged SiC BJT [102] became available near the time completion of the research and was retrospectively added.

Transistor	**Type**	**Max $T_{junction}$**	**$R_{thermal,Junction-Case}$**
CMF10120D	MOSFET	150°C	0.4°/W
SJEP120R125 [Appendix C]	EM JFET	175°C	1.1°/W
SJDP120R045 [91]	Normally-on JFET	150°C	0.6°/W
BitSiC1206 [75]	BJT	225°C	0.5°/W [102]

Table 3-4: Maximum junction temperatures and thermal impedances of SiC transistors in TO-247 cases

The maximum power dissipation for each device was then calculated for a range of case temperatures as shown in Figure 3-2. The SiC BJT clearly exhibits superior power dissipation any case temperature due to its much higher permissible junction temperature.

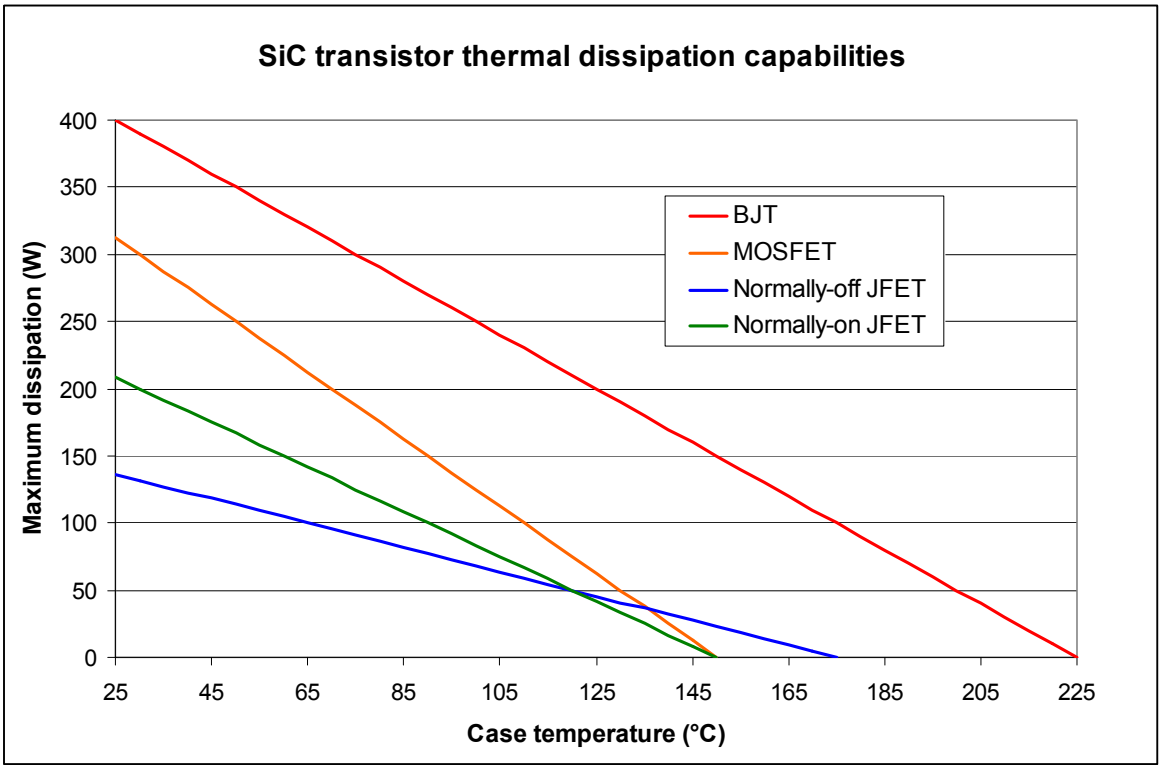


Figure 3-2: Thermal dissipation capabilities of SiC transistors

3.9 Choice of transistor for further research

Because the research in this thesis was conducted in collaboration with industry, the choice of device for further analysis must be made by incorporating business priorities as well as academic and technical considerations. The proposition of using normally-on transistors as the primary blocking device on the input of a commercial telecommunications power converter was perceived as too large a business risk to pursue at the time. This ruled out the use of the SJDP120R045 normally-on JFET.

The potential for the BitSiC1206 to operate with junction temperatures of up to 225°C was considered to be a good opportunity to move toward smaller, cheaper heatsinks in telecommunications rectifiers and possibly allow the use of passive cooling. While conduction losses for the BitSiC1206 were not as good as those of the MOSFET or JFETs, it was anticipated that BJTs would soon become available with higher current ratings. The

saturation voltages of these BJTs were expected to compare favourably against the ohmic channel resistance losses exhibited by the MOSFET and JFETs.

Some initial research was performed to determine whether or not switching losses in SiC BJTs could be reduced by connecting a low voltage silicon MOSFET in cascode. At the time of the initial research, the BitSiC1206 was not yet commercially available. Private communications with Transic led to a price of €650 per transistor being quoted for samples from their laboratory facility. This was outside of the budgetary constraints of the project. The results that had been obtained at the time using silicon BJTs are described in Appendix A.

Having ruled out the normally-on JFET and BJT, a final decision was made to focus on the SemiSouth SJEP120R125 EM JFET rather than the Cree CMF10120D MOSFET. This decision was based partly on the expectation that the EM JFET's switching performance would allow higher switching frequencies to be achieved than with the MOSFET. The maximization of switching frequency is a major business objective because it allows the use of smaller capacitors and inductors. Inductors and capacitors with smaller values are both cheaper and physically smaller, allowing the physical size and profit margin objectives of the business to be more easily met.

The main drawback of choosing the EM JFET is that its conduction losses are highly temperature dependant, posing a risk of thermal runaway. Because fan-forced cooling is relatively ubiquitous in telecommunications power converters, it is expected that the temperature of the SJEP120R125's case can be kept sufficiently low to prevent conduction losses from becoming unreasonably high.

3.10 Gate drives for EM SiC JFETs

Having chosen Semisouth's EM SiC JFETs for further research, an important aspect to consider is their gate drive requirements. Although the EM JFET is a voltage controlled device, current flows through the gate-source junction in the presence of a gate-source voltage [37]. This makes the EM SiC JFET more like a BJT than a MOSFET from a driver perspective.

At the commencement of the research in this thesis, few gate drive circuits had been proposed for the EM SiC JFET. In [98], modifications were made to the IGBT drive circuit shown in Figure 3-3 (left), to accommodate an EM SiC JFET as shown in Figure 3-3 (right). The value of R1 was increased to limit the sustained gate current and C1 was added to improve the turn-on and turn-off times of the EM SiC JFET.

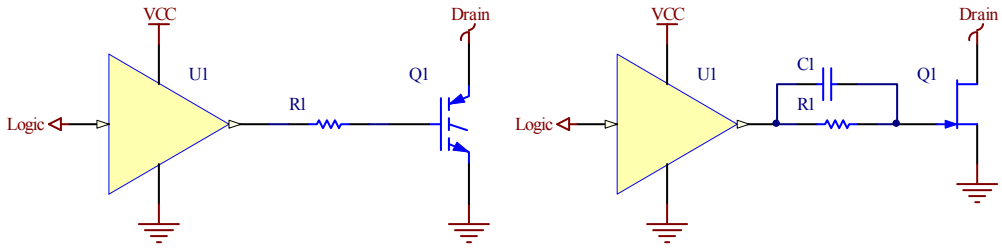


Figure 3-3: The IGBT driver circuit (left) is modified to accommodate an EM SiC JFET (right)

A speedup capacitor was also used in parallel with a series gate resistance in [97] however, an amplifier with a push-pull output stage was also used to achieve a sustained low-impedance negative gate-source voltage at turn-off. The use of a bipolar driver was also being advocated in the edition of the SJEP120R125 datasheet available at the time [103]. These developments form a starting point for Chapter 5, where an implementation is presented for a bipolar EM SiC JFET driver. The same building blocks are used as those found in MOSFET driver ICs to demonstrate the feasibility of fabricating an integrated circuit for driving EM SiC JFETs. The proposed driver features a built-in charge-pump circuit to generate its own negative supply rail and a special bootstrap arrangement to level-shift the split supply rail up to the high side drive.

During the period of the research in this thesis, SemiSouth developed an improved EM SiC JFET driver circuit using a two-stage DC-coupled bipolar output [104]. This driver delivers a high-current turn-on pulse followed by a smaller sustained gate current without the need for a speedup capacitor. The two-stage driver delivers more precise control over the gate current of the SiC JFET and claims to achieve better switching performance than AC coupled circuits.

The two-stage DC-coupled design lacks the ability to operate from one single-ended power supply, requiring a pair of split supplies. This constraint is easily solved in a laboratory context, so the driver was adopted for the PFC in Chapter 6 through to Chapter 8. When adapting a commercial product for EM SiC JFETs, the requirement for a pair of split

auxiliary power supplies is more of a constraint, and the charge-pump and bootstrap proposed in Chapter 5 could be combined with the DC coupled output from [104] to achieve a particularly attractive solution.

Several other notable advances were also published in the literature after the completion of the research in Chapter 5 in 2009. In particular, an updated paper on the two-stage driver was published [105] as well as a reference circuit based on it [106]. Meanwhile, other researchers published an integrated circuit for driving EM SiC JFETs [107].

3.11 Conclusions

A range of SiC transistors were considered including MESFETs, MOSFETs, normally-on JFETs, normally-off JFETs and BJTs. Using the information available during the early stages of the research covered in this thesis, comparisons were made for the expected conduction losses, switching losses and thermal performance of each device.

The SJEP120R125 normally-off JFET had a lower calculated conduction loss than the CMF10120D MOSFET at 25°C but higher at 150°C. The BitSiC1206 BJT had the highest conduction loss of all the transistors considered despite having the smallest maximum current rating.

When comparing switching losses, the data available for each transistor was measured by their respective manufacturers under differing conditions, however a rough comparison was possible. The SJEP120R125 normally-off JFET appeared to offer the best switching performance followed by the BitSiC1206 BJT with the CMF10120D MOSFET exhibiting approximately double the turn-off energy of the SJEP120R125 under similar conditions. Switching energy data was not available at the time for the SJDP120R045 normally-on JFET.

The thermal impedances of the SiC transistors were then compared as well as their maximum junction temperature ratings. The amount of power that each transistor was expected to be able to dissipate was computed as a function of case temperature. The BitSiC1206 BJT was expected to be capable of the highest power dissipation due to its much higher allowable junction temperature of 225°C compared to those of the JFETs and

MOSFET. With case temperatures below 135°C, the CMF10120D MOSFET exhibited a higher dissipation capability than either of the JFETs while the normally-off JFET performed worse than all of the other transistors for case temperatures of less than 120°C. The SJEP120R125 normally-off JFET is expected to be able to dissipate more power than the SJDP120R045 normally-on JFET or CMF10120D MOSFET at case temperatures in excess of 135°C because of the SJEP120R125's 175°C junction temperature rating.

The methodology behind the selection of a transistor for most of the research in this thesis to focus on was presented. Business priorities including higher switching frequency, smaller heatsinks and the use of normally-off devices were considered. Technical aspects such as switching losses, conduction losses and thermal dissipation capabilities were also considered as well as research budget. The aspects were then weighed up and the decision made that the SJEP120R125 EM SiC JFET will be the focus of ongoing research.

Finally, circuits suitable for driving EM SiC JFETs were discussed. The timeline of key developments of knowledge in the literature about the driving of EM SiC JFETs was discussed, providing context for the research in Chapter 5.

Chapter 4 SJEP120R125 SiC JFET

In 0, EM SiC JFETs were selected as the focus of further research. SemiSouth's first commercially available EM SiC JFET is the SJEP120R125, which became commercially available in 2008, near the start of the research in this thesis. Because this transistor was particularly new, limited technical information was available, making its integration into telecommunications power converters challenging. In this chapter, the characteristics of the SJEP120R125 that were known about at the time are presented as well as a series of tests conducted by the author to further characterize the device.

Specifically, assumptions that the SiC JFET cannot block in reverse due to its structure were tested, as well as its passive and active rectification characteristics. Important new discoveries were made about the gate characteristics of the SJEP120R125 in synchronous rectification circuits. These characteristics have a significant impact on the drive losses associated with synchronous rectification with the SJEP120R125.

4.1 Background

The SJEP120R125 utilizes a vertical or 'trench' architecture as shown in Figure 4-1 [108]. Unlike many JFETs, the SJEP120R125 is able to block significant drain-source voltages without any gate-source voltage (characteristic of power MOSFETs), because of its unique semiconductor design. The SJEP120R125 has a $R_{DS(on)}$ of 125mΩ [Appendix C] and a blocking voltage of 1200V. Despite the low $R_{DS(on)}$, the SJEP120R125 also has a very low input capacitance of 610pF at a V_{DS} of 100V. This suggests that it should be possible to turn the SJEP120R125 on and off very rapidly.

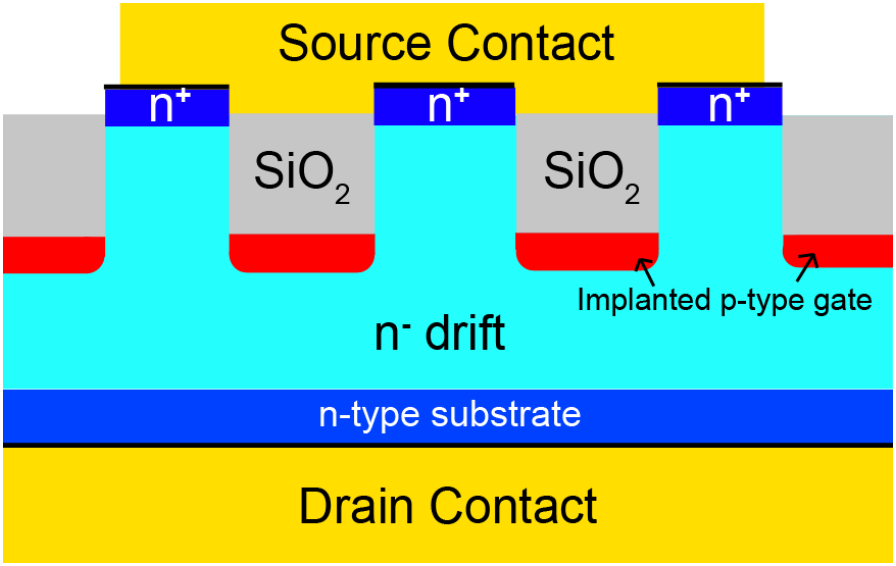


Figure 4-1: The SJEP120R125 SiC JFET's structure

Fifteen sample SJEP120R125 JFETs were obtained and five were utilized in the circuits presented in this chapter to evaluate the potential for their introduction into telecommunications power converters. Statistical analysis of variations between individual transistors were not performed owing to the following reasons. As the samples came from the same batch, there will not be the variation expected from transistors from separate batches. There was also a perceived lack of commercial value in undertaking such an analysis, compared to the value of uncovering the overall trends for a larger range of the JFETs' previously unpublished characteristics ahead of competitors. Additionally, the transistors must be able to work in potential commercial products irrespective of transistor-to-transistor variations, and as such, the investigations and developments utilizing the sample JFETs have been made with an attempt to be robust against such variations.

The DC tests in Section 4.2 confirm the author's expectation that a normally-off SiC JFET's channel can conduct in either direction and only blocks high voltage in one direction. In Section 4.2.4, a previously unknown gate current characteristic is discovered which has significance when designing SiC JFET drive circuits.

In a private communication between Semisouth and the author at the time of research and later in [108], it was confirmed by Semisouth that the SJEP120R125 does not contain a body diode. Despite this, its drain-source capacitance will allow some current to flow while the drain-source voltage rises when transitioning from reverse conduction (source to drain direction) to a forward blocking state. The reverse recovery-like characteristics of the

SJEP120R125 are measured and compared to those of silicon and silicon carbide diodes in Section 4.3.1 to gain an understanding of the performance of the SJEP120R125 as a passive rectifier. Finally, a synchronous rectification circuit is constructed in Section 4.3.2 to evaluate the SJEP120R125's operation as an active rectifier.

4.2 DC tests

In many applications current needs to flow in the reverse direction from source to drain in N type transistors, as for example, in synchronous rectification circuits. The SJEP120R125 datasheet [Appendix C] neglects to mention reverse conduction characteristics, but based on the behaviour of other JFETs, it is hypothesised that the SJEP120R125 will conduct in reverse when biased on. The reverse blocking capabilities of the SJEP120R125 (if any) are unclear from the available information, though the manufacturer has stated that, unlike MOSFETs, the SJEP120R125 does not contain a parasitic body diode [104].

4.2.1 Reverse conduction

To better understand the reverse characteristics of the SJEP120R125, several DC tests were performed using the circuit shown in Figure 4-2. Voltage source V1 allows the gate-source voltage to be controlled, while V2 and R1 provide a source-drain current for Q1. The polarity of V1 can also be reversed to measure under negative gate bias conditions.

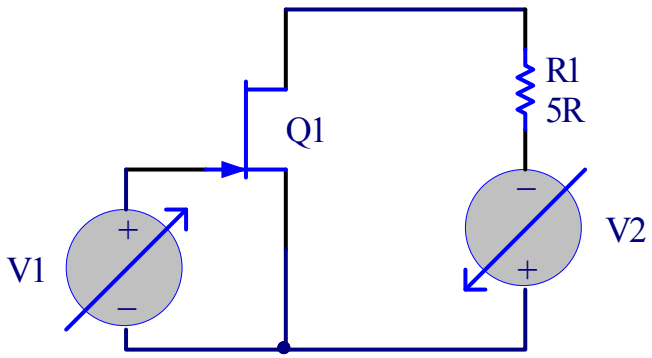


Figure 4-2: The test circuit used to determine the reverse DC characteristics of the SJEP120R125

V1 and V2 were varied over a range of values to observe the reverse conduction characteristics of the SJEP120R125. Tests were performed at room temperature (22°C ambient) with the SJEP120R125 bolted to a large heatsink (0.5°C/W) to minimise self

heating effects. The heatsink was fan-forced and a silicone heat transfer compound was used between the mating faces of the heatsink and transistor case.

The measurements plotted in Figure 4-3 demonstrate that the SJEP120R125 is able to conduct in either direction. The channel conducts better in the reverse (source to drain) direction at low gate-source voltages than in the forward direction. The difference between forward and reverse conduction is much larger with a gate-source voltage of 2.0V, where thermal runaway consistently occurred when a forward current larger than 6A flowed despite fan-forced cooling. Meanwhile with a gate-source voltage of 3.0V, conduction was almost identical in either direction for drain currents up to 12A. Voltage and current measurements were made using Fluke 79 true-RMS multi-meters. Voltage measurements have an accuracy of 0.3% ± 3mV and the current measurements have an accuracy of 0.5% ± 20mA.

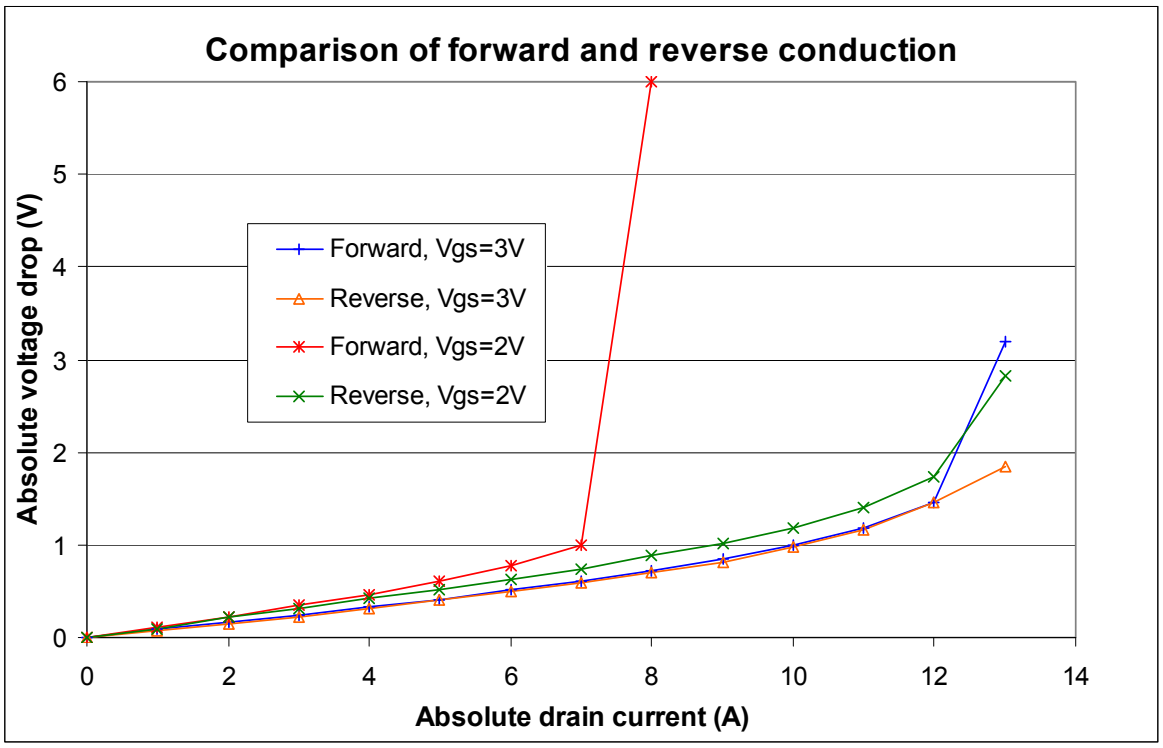


Figure 4-3: The SJEP120R125 conducts well both forward (conventional current flowing drain to source) and in reverse (conventional current flowing source to drain)

It was anticipated that bidirectional conduction would be possible with some difference between forward and reverse conduction occurring based on the schematic representation of the EM SiC JFET in [104], reproduced in Figure 4-4. When channel current is flowing in the drain to source direction, the voltage drop across R_S causes the voltage appearing

across the gate-source diode to be less than the gate-source terminal voltage. Conversely, when current flows through the channel in the source to drain direction, the voltage drop across R_S causes the voltage drop across the gate-source diode to be larger than the gate-source terminal voltage. As the gate-source terminal voltage is increased, the voltage drop across R_S represents a smaller proportion of the gate-source diode voltage, causing the effect to become less pronounced, as observed in Figure 4-3 when going from 2V to 3V.

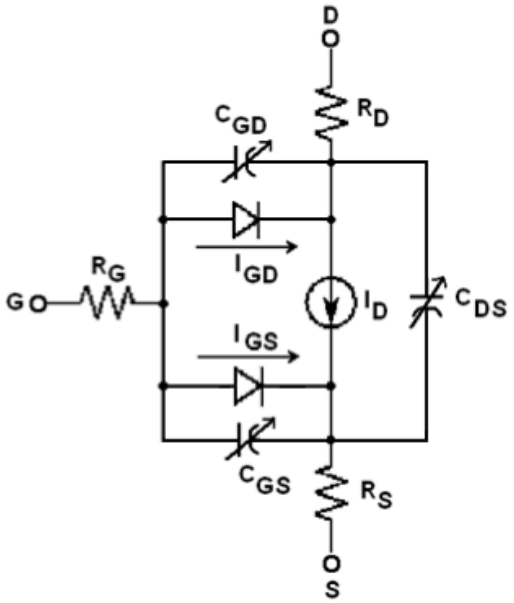


Figure 4-4: JFET equivalent circuit, reproduced from [104]

4.2.2 Reverse blocking ability

The reverse blocking ability of the SJEP120R125 was tested by varying V2 with the gate and source short-circuited. As shown on the blue curve in Figure 4-5, the reverse blocking voltage appears to be just short of one volt. Applying a negative gate-source bias causes the reverse blocking voltage to increase by a similar magnitude, as shown in Figure 4-5.

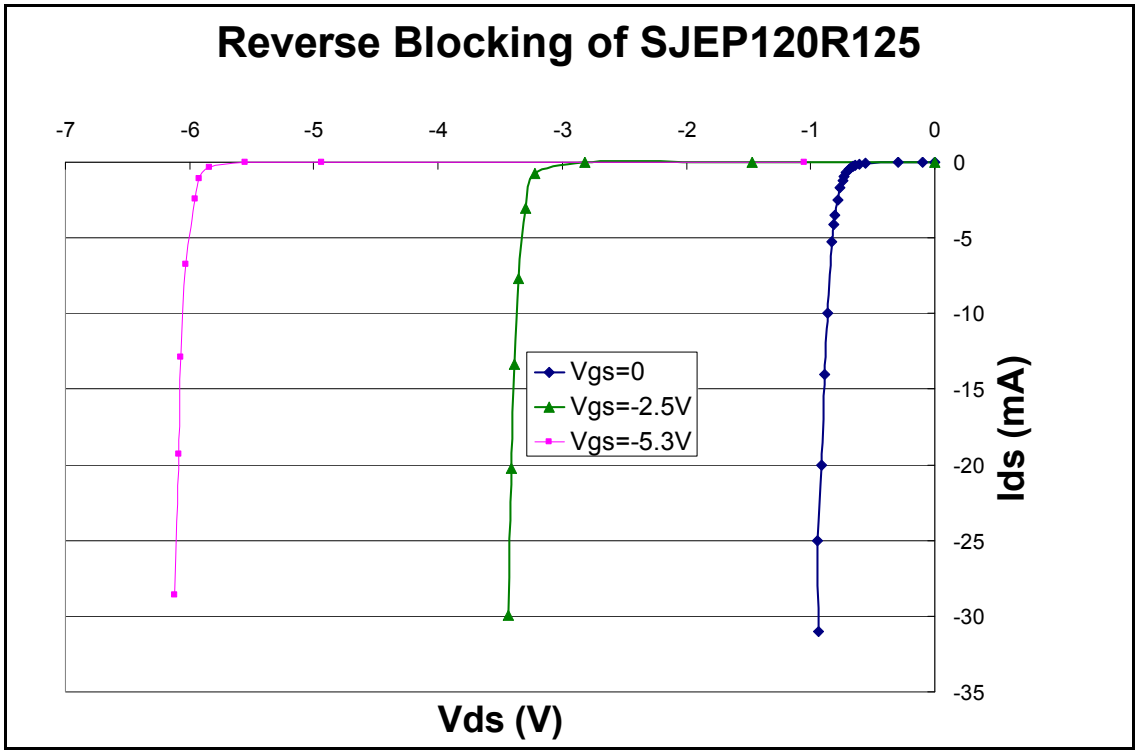


Figure 4-5: Reverse blocking characteristics of the SJEP120R125

The reverse blocking ability of the SJEP120R125 is minimal, but can be increased by applying a negative gate-source voltage. Therefore, the SJEP120R125 is suitable for use with a fast external anti-parallel diode, because its reverse blocking voltage is controllable. This is a feature that is not available with many silicon MOSFETs because they contain parasitic body diodes. MOSFET body diodes usually exhibit very low forward voltage drops. This makes it impractical to connect faster external diodes in parallel with them, resulting in their often poor reverse recovery characteristics that limit the dynamic performance of some applications.

Even in situations where a combination of MOSFET and external anti-parallel diode can be found that meets the forward voltage drop constraints, parasitic inductance can severely limit any improvement [109, 110]. Therefore, if the option of an anti-parallel diode was to be pursued with the SiC JFET, it would ideally be co-packaged with the SiC JFET to minimize the parasitic inductance between the transistor and diode.

4.2.3 Characteristics near the boundaries of thermal runaway

As drain current is increased through the SJEP120R125, thermal dissipation rises nonlinearly because the channel resistance increases with temperature. At some dissipation

level, dependent on the particular thermal circuit, a thermal runaway occurs. The SJEP120R125 was tested to thermal runaway using a 0.5°C/W heat sink with forced air cooling at an ambient temperature of 22°C. The characteristics observed are shown in Figure 4-6. With a gate-source voltage of 3.0V, thermal runaway occurred with positive drain-source currents in the range of 12-13A. It is important to note that in circuits with a higher thermal impedance or ambient temperature, V_{DS} will be larger and thermal runaway will be reached at a lower drain-source current.

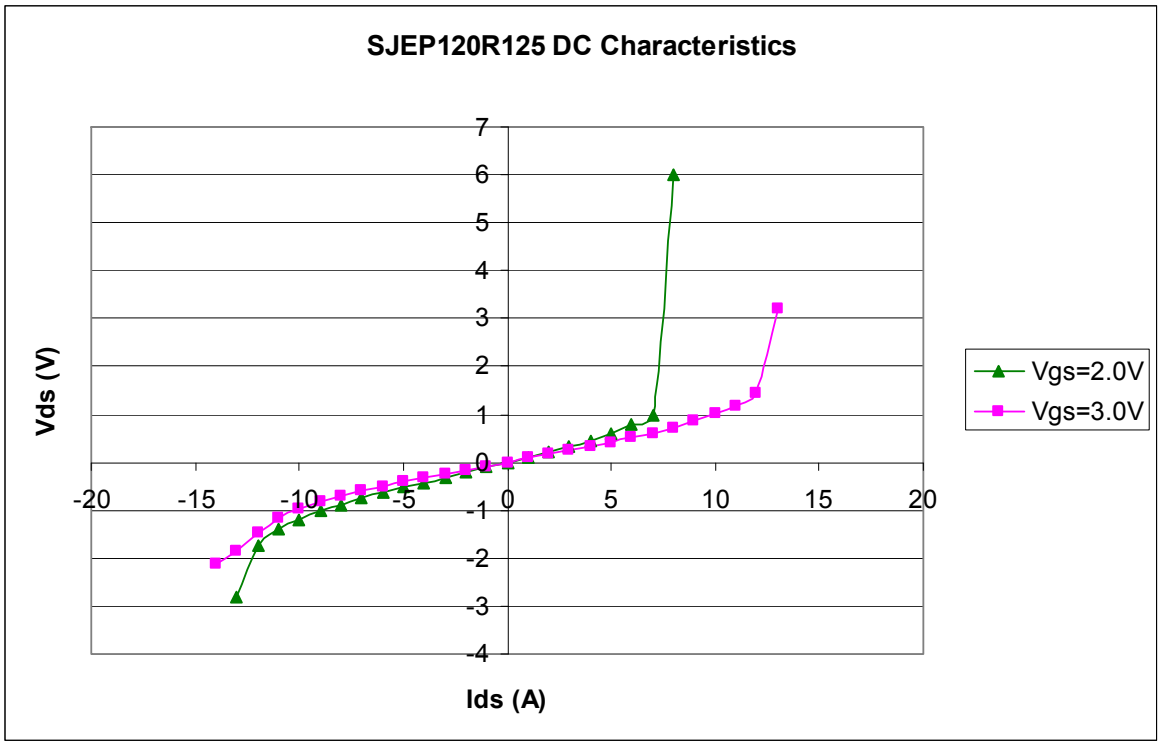


Figure 4-6: SJEP120R125 Characteristics showing thermal runaway

4.2.4 Drive power

While testing the SJEP120R125's ability to conduct in both forward and reverse directions, it was observed that particularly large gate currents flowed when the channel was conducting in the source to drain direction. Details of this characteristic for the SJEP120R125 were not found in the literature. The characteristic was measured over a wide range and is shown in Figure 4-7. The gate current can be seen rising sharply when the drain current is larger than 10A in the source to drain direction. Similar sized drain to source currents did not correlate with a steep increase in gate current. Instead, the gate current remains below 250mA up to the point of thermal runaway.

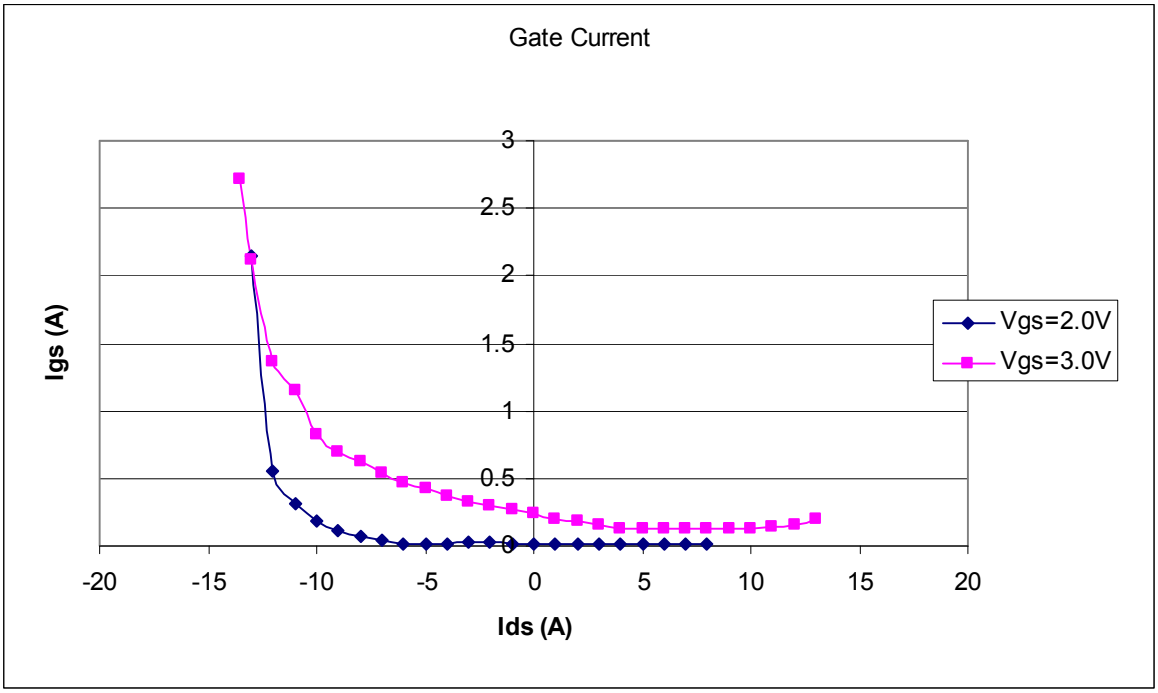


Figure 4-7: SJEP120R125 gate current draw under fixed gate-voltage conditions

With a gate voltage of 3V and a source to drain current of 14A, the SJEP120R125 draws a gate current of 2.75A. This represents a drive loss of 8.25W which is approximately 20% of the channel conduction losses under these conditions. 2.75A of continuous gate current is wasteful and would require a powerful gate drive circuit. Considering the normally-off SiC JFET's electrical model in Figure 4-4 it is not entirely clear what effects may result from negative values of I_D. One possibility is that a small voltage drop appears across I_D in Figure 4-4 resulting in most of the gate current comprising of I_{GD} instead of I_{GS}. This in turn could result in the need for a much larger gate current, in order to have a large enough I_{GS} for the JFET to achieve an acceptably low $R_{DS(on)}$. The absolute value of V_{DS} was less than 1V for currents of up to 13A in either direction,

Further tests were conducted to observe the effects of limiting the SJEP120R125's gate current to a more appropriate arbitrary magnitude. A limit of 250mA was chosen because it is slightly larger than any gate current observed during forward conduction. The test was repeated with zero gate current as a further comparison to verify that synchronous rectification is indeed beneficial with the SJEP120R125. The results of these tests are shown together in Figure 4-8. It may be concluded that performing synchronous rectification with the SJEP120R125 is beneficial, because the reduction in channel voltage when biased on is significant. With a 250mA current limit, most of this advantage can be

attained for source-drain currents of less than 11A. If source to drain currents in excess of 11A are expected, a diode connected in anti-parallel will offer a lower voltage drop than the SJEP120R125 without the excessive drive losses that would result from driving the gate with a 3V constant voltage bias.

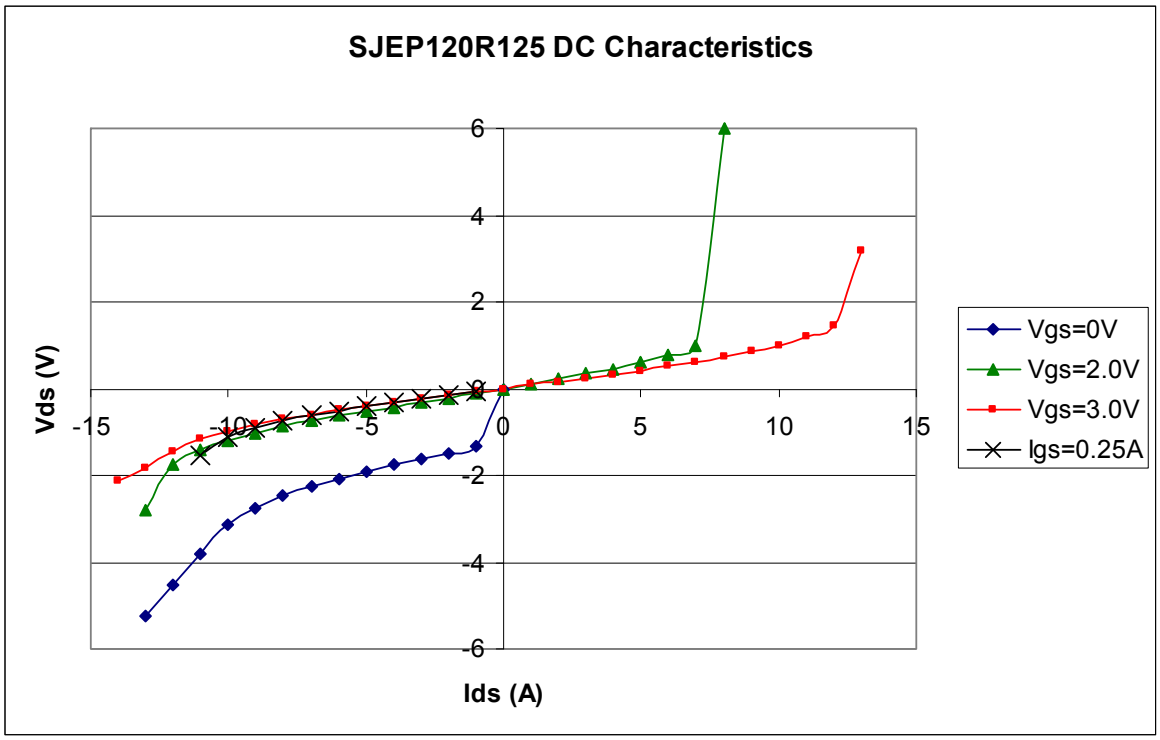


Figure 4-8: SJEP120R125 characteristics over a broad range for a variety of biasing conditions

4.3 AC tests

4.3.1 Reverse recovery of the SJEP120R125

Although the ability to block several volts in reverse allows the SJEP120R125 to force a fast anti-parallel diode to conduct, the parasitic capacitances of the SJEP120R125 are still present and will an effect on the switching characteristics of the external diode. To test the effect of these capacitances, a reverse recovery test was devised, similar to [111].

A buck converter with a high-side switch was chosen for the test circuit because it allows the freewheeling diode (in this case a SJEP120R125 under test) to have one of its terminals connected to ground, making its high $\frac{dv}{dt}$ voltage easy to observe with a single high-bandwidth oscilloscope probe. A gate-source bias can also be applied from a standard

power supply if desired, because the source terminal of the SJEP120R125 is connected to the low $\frac{dv}{dt}$ ground node. The test circuit is shown in Figure 4-9, where Q1 is the high side PWM switch while Q2 is the device under test (DUT).

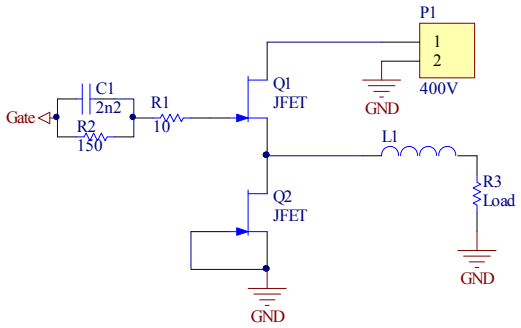


Figure 4-9: The reverse recovery test circuit

JFET Q1 in Figure 4-9 is driven by a commercial MOSFET driver, U2 as shown in Figure 4-10. A PWM signal is applied to P2 which is isolated from U2 and Q1 by optical isolator U1. The full test circuit including decoupling capacitors and ancillary components is provided in Appendix B, Schematic 1. R2 was selected to limit the continuous gate current to approximately 40mA, to ensure that Q1 would saturate at the load current of approximately 4A, based on the characteristic curves in the SJEP120R125 datasheet [Appendix C]. With a supply voltage of 9V and an assumed gate-source voltage drop of 3V, when the charge-pump effect is taken into account, C1 sees a voltage swing of 12V. The value of 2.2nF was chosen for C1 to achieve a charge transfer of 26.4nC, closely matching the 25nC gate charge of Q1. The sustained gate current is then set at approximately 35mA by R1 and R2.

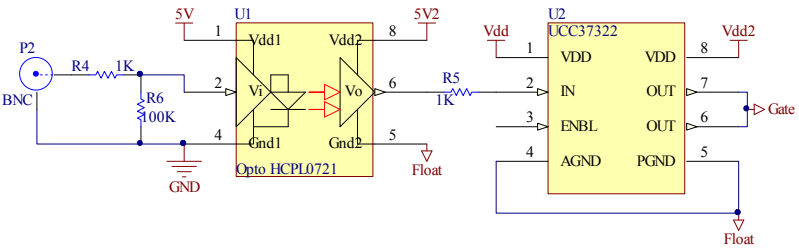


Figure 4-10: The reverse recovery test-bed's gate drive circuitry

Applying a short pulse to P2 allows the reverse recovery of the DUT to be observed. The JEDEC standard for measuring reverse recovery of power MOSFETs [111] provides

sample waveforms, demonstrating the standard methods for calculating *trr*. By following these guidelines, *ta*, the time between the current through the device under test reaching zero and the reverse current overshoot peak is measured as being 18.0ns, as shown in Figure 4-11 for the SJEP120R125. To calculate *tb*, the time between the reverse current reaching its peak of 2.35A and falling to 0.25 of the peak value must be measured, in this case, 15.0ns. If a linear approximation of these two points is created, a zero crossing occurs at 20ns. Therefore, *tb* is 20ns and the reverse recovery time (*trr*) of the SJEP120R125 is calculated by summing *ta* and *tb*.

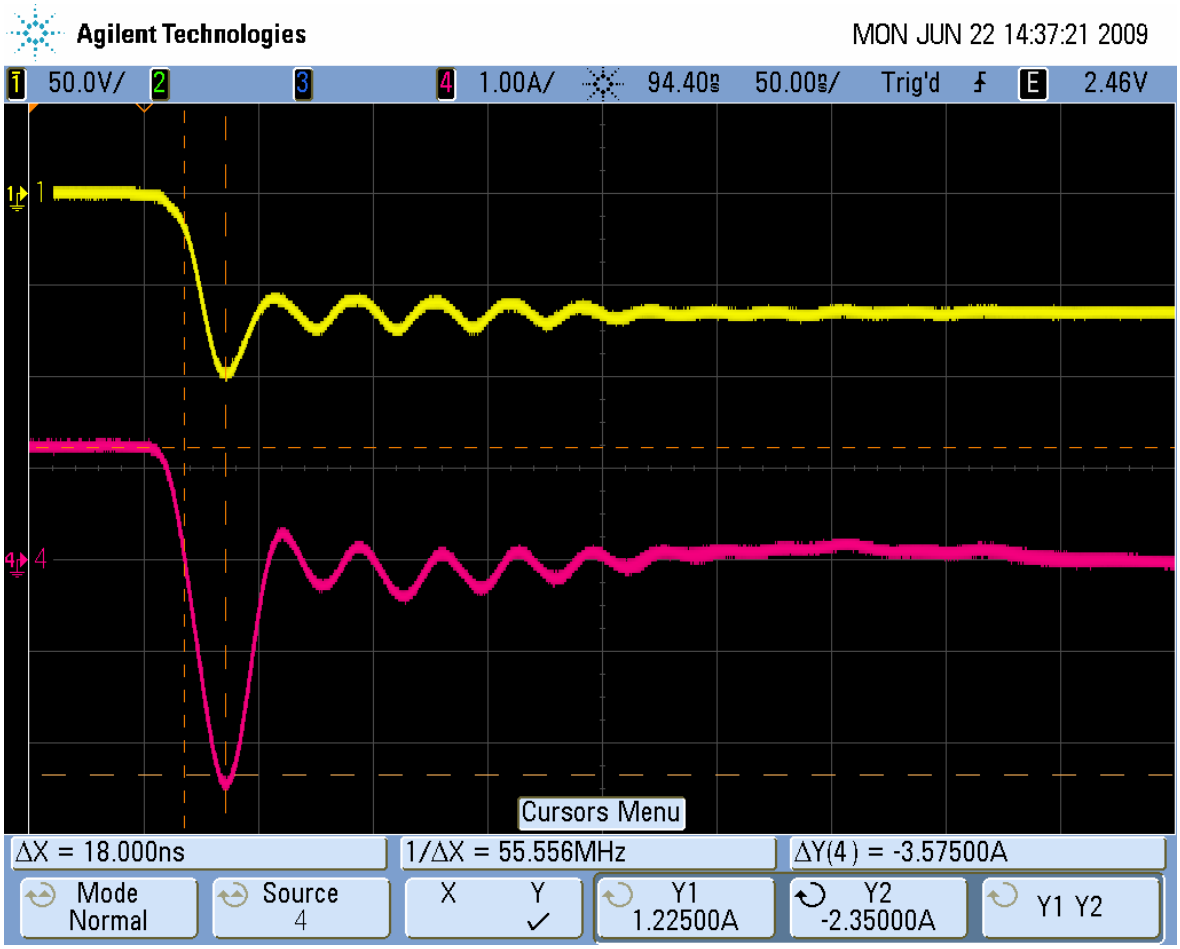


Figure 4-11: Measurement of *ta*, the time from the current (channel 4, pink) crossing zero to the peak reverse current, for the SJEP120R125 normally-on SiC JFET. (Source-drain voltage - channel 1, yellow is not needed for the *trr* calculations).

To provide a fair comparison, the same test conditions are repeated with an IPW60R099CP silicon MOSFET (chosen for its similar channel resistance to that of the SJEP120R125), a RHRP1560 hyper-fast silicon diode (chosen for its similar current rating to the SJEP120R125), a SDT10S120 SiC Schottky diode (chosen for its similar voltage rating to

the SJEP120R125) as well as the combination of a SJEP120R125 and a SDT10S120 connected in anti-parallel. The results of these tests are summarized in Table 4-1.

Part number	Part Type	*ta* (ns)	*tb* (ns)	*trr* (ns)
SJEP120R125	SiC JFET	18.0	20.0	38.0
IPW60R099	Si MOSFET	140.0	29.3	169.3
RHRP1560	Si Hyperfast diode	14.6	9.9	24.5
SDT10S120	SiC Schottky diode	13.6	9.1	22.7
SJEP120R125+SDT10S120	SiC JFET+SiC diode	23.0	22.9	45.9

Table 4-1: Summary of reverse recovery tests for different diodes

The reverse recovery characteristics of the SJEP120R125 SiC JFET are significantly better than those of the IPW60R099 silicon MOSFET and the addition of an anti-parallel diode results in better performance than the sum of the JFET and diode's separate reverse recovery times. During the reverse recovery tests that included a SiC JFET, the JFET's gate and source were tied together. DC tests demonstrated that the SiC JFET has a significantly larger voltage drop than either diode at 2.35A. This means that in the reverse recovery tests where a JFET was connected in anti-parallel with an external diode, conduction did not occur through the JFET.

The results show that the SJEP120R125 should perform well in high speed, hard-switched applications and that a high speed diode can be connected in anti-parallel without its performance being unreasonably compromised by the SJEP120R125's parasitic capacitances.

4.3.2 Synchronous rectification performance of the SJEP120R125

Having shown that the SJEP120R125 achieves good DC conduction performance as well as fast reverse recovery times, it is highly likely that it will perform well in synchronous rectification circuits. A synchronous rectification circuit, shown in Figure 4-12 was designed to measure the SJEP120R125's performance in synchronous rectification applications. Q1 is the device under test, while Q2 acts as a switch. The circuit allows for Q1 to have an optional high speed diode connected in anti-parallel in the position marked by D1.

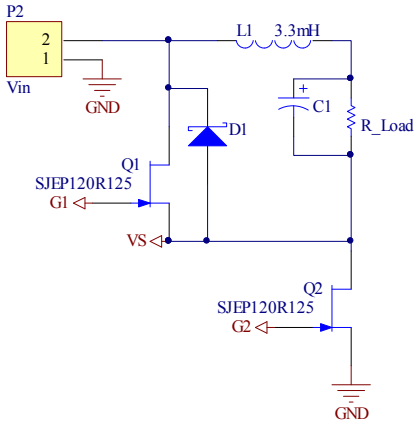


Figure 4-12: Synchronous rectification test circuit

The drive circuit is built around an IRS21844 MOSFET driver, configured as shown in Figure 4-13. The IRS21844 has a variable dead time that is adjustable via R7 to prevent shoot-through conditions from occurring. Battery BT1 provides a simple floating power supply for Q1, suitable for this transistor characterisation circuit. The nominal voltage of BT1 was 9V and remained above 8.8V throughout the tests. In a commercial product, a bootstrap circuit would be used here or alternatively an isolated power supply such as a small flyback converter. The gate drive power supplied by the batteries (6x AA) was not included in the efficiency calculations. Resistors R2 and R6 limit the continuous gate current of each JFET to approximately 200mA, while capacitors C2 and C3 allow a much higher current to flow briefly at turn-on and turn-off because of their low dynamic impedance and charge pump effect. A 50% duty cycle PWM signal is connected to P1 with sufficiently high frequency to achieve continuous conduction in L1. Continuous conduction simplifies circuit control by allowing Q1 to simply be turned on whenever Q2 is off.

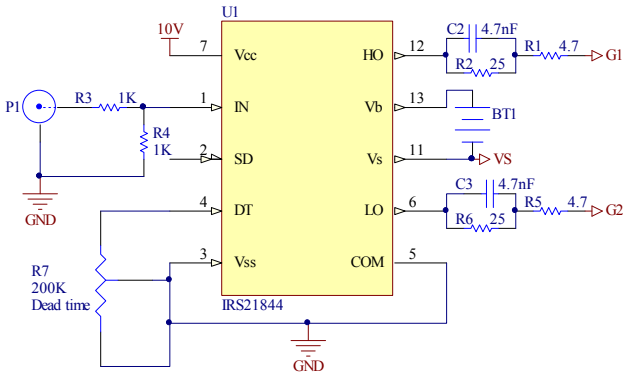


Figure 4-13: Overview of the drive circuit for the synchronous rectification test circuit

The complete synchronous rectification circuit including test points and decoupling is shown in Appendix B, Schematic 2 and was constructed on a PCB as shown in Figure 4-14. The IRS21844 MOSFET driver is not visible as it is surface mounted on the copper side between the two transistors to minimize gate drive loop areas.

Figure 4-14: Synchronous rectification test circuit.

Shoot-through problems were observed while testing the synchronous rectification circuit despite the use of a particularly large dead time of 400ns between Q1 turning off and Q2 turning on. The shoot-through was observed starting at the same instant that Q2 turned on and lasted for 1.5ns. The shoot-through was caused by Q1 failing to remain off while Q2 turns on. When Q2 turns on, the voltage on the midpoint of the half bridge (connected to Q1's source) falls very rapidly. For Q1 to remain off, its gate voltage must fall at the same rate as its source voltage. As the drain-source voltage across Q1 increases, Q1's drain-gate and gate-source capacitances form a capacitive divider with Q1's gate at the centre point. Although the gate drive circuit should maintain a short circuit between Q1's gate and source, it is inevitable that this short circuit has some stray inductance, across which a voltage sufficient to turn on Q1 is briefly developed. Adding additional gate-source capacitance can alleviate the problem but has a detrimental effect on switching speed. A better solution is to hold the gate voltage several volts below the source voltage so that a much larger voltage must be developed across any parasitic inductances before Q1 can turn on.

Connecting a diode in series with Q1's source as shown in Figure 4-15 raises the source voltage with respect to the VS terminal of U1 by one diode voltage drop. This allows the gate of Q1 to be pulled below the source voltage when U1 pulls G1 to VS. Pull-up resistor

R18 was also added to keep D4 forward biased at all times. Because the inductive load is connected on the anode side of D4, synchronous rectification is not blocked by D4. The use of a series diode is not a suitable solution for all applications because of the additional conduction losses that it introduces, but it eliminated shoot-through in the test circuit without interfering with other circuit parameters. This allowed a fair comparison to be made between synchronous rectification and passive rectification of the SJEP120R125.

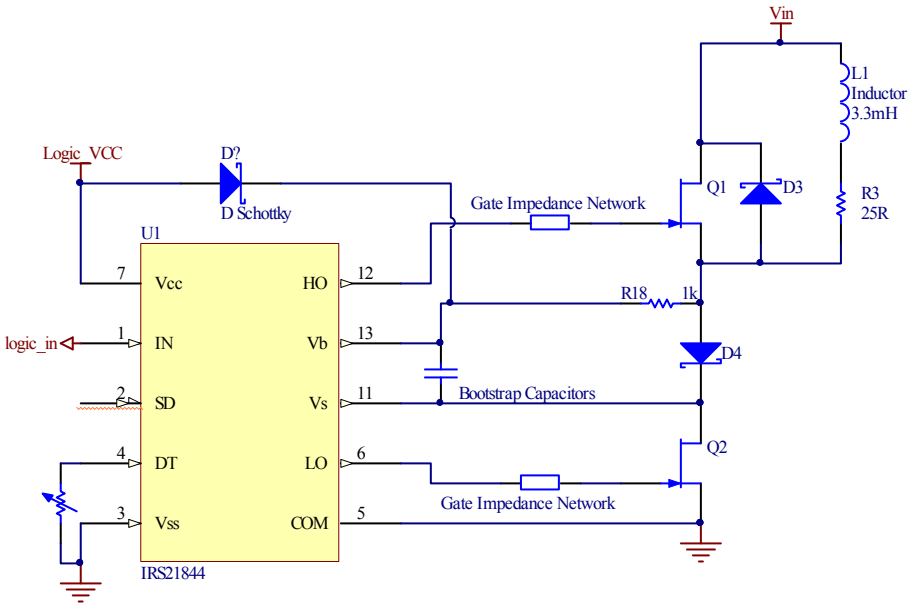


Figure 4-15: Simplified schematic showing the addition of a diode in location D4 to raise Q1's source terminal relative to the Vs terminal of U1.

The input of the buck converter was connected to a DC power source with a measured voltage of 126.0V and the output of the converter was connected to a resistive load of 13.0Ω. The load was connected in series with a large inductance of 3.3mH to minimize 100kHz current ripple. The input and output voltages and currents were measured using Fluke 79 multi-meters. The measurement accuracy of the meters was 0.3% ± 200mV for the voltage measurements, 0.5% ± 5mA for the input current measurements and 0.5% ± 20mA for the output current measurements. Each operating point was allowed to thermally stabilise for 5 minutes at which point multiple concordant readings were achieved. Table 4-2 shows a summary of the measurements and demonstrates that a 0.6% higher electrical efficiency was achieved when synchronous rectification was enabled compared to when the SJEP120R125 was used with an external rectifier diode.

Rectifier:	V_{in}	I_{in}	V_{out}	I_{out}	P_{loss}	Efficiency
Synchronous SiC JFET	126.3V	1.971A	54.7V	4.18A	20.3	91.8%
RHRP1560 diode	126.0V	1.991A	54.6V	4.19A	22.1	91.2%

Table 4-2: Performance of a pair of SJEP120R125 SiC JFETs in a buck converter with synchronous rectification enabled or disabled.

Static tests found that the voltage drop of the SJEP120R125 with a source to drain current of 4.2A to be 0.31V with a gate-source voltage of 3.0V. The external anti-parallel diode (RHRP1560) was found to have a forward voltage drop of 1.2V at 4.2A. This is lower than the voltage drop of the SJEP120R125 with a gate-source voltage of zero. The expected difference in losses based on these measurements, with a 50% duty cycle, is 1.9W. This is in close agreement with the measured saving of 1.8W. Although the SJEP120R125 achieved higher efficiency when synchronous rectification was enabled than when relying on the anti-parallel RHRP1560 diode, the improvement was smaller than the accuracy of the measurements. Therefore, whilst it has been demonstrated that synchronous rectification is possible with the SJEP120R125, it is not necessarily beneficial under all conditions. The drive losses, calculated at approximately 0.6W will also further reduce the difference.

4.4 Summary

Some of the reverse blocking and gate current characteristics discovered via testing as detailed in this chapter had not been previously published and are of material interest in the design of any circuit where reverse conduction will occur through normally-off SiC JFETs. Specifically, the large gate currents that are drawn by the normally-off SiC JFETs when current flows in the source to drain direction were not known about at the time of testing. Furthermore, the demonstration that an overall performance improvement can be achieved by significantly limiting the gate current during negative drain-source currents flows was not previously known. These new findings were presented by the author in [9].

Although the SJEP120R125 does not have a body diode, it will still exhibit reverse recovery-like characteristics due to its parasitic capacitances. If the SJEP120R125 is biased off and its drain source voltage allowed to rise, current will flow during the rise through the SJEP120R125's drain-source capacitance. Similarly, the gate-drain capacitance will carry some current when the drain-gate potential changes. These currents flowing during increasing drain-source voltage are similar to the reverse recovery of a MOSFET body

diode, where current flows during the depletion of charge from the diode's junction. In a bridge topology, it does not matter whether the effect is due to diode recovery or parasitic capacitances: the result is a loss. To quantify the reverse recovery-like characteristics of the SJEP120R125, the effects of its parasitic capacitances were measured and compared to the reverse recovery performance of a silicon hyper-fast diode, a silicon carbide Schottky diodes and the body diode of a silicon MOSFET. It was found that the SJEP120R125 achieves rectification performance that is within a factor of two of the performance achieved by the diodes and almost an order of magnitude better than that of the silicon MOSFET's body diode. Because of this and the results of testing in the synchronous rectification application in 4.3.2, it is concluded that the SJEP120R125 has better dynamic performance for synchronous rectification than the similarly rated MOSFETs it was compared to. At current levels of approximately 4A, the SJEP120R125 exhibits similar losses when used as a synchronous rectifier to those dissipated by a passive RHRP1560 diode. At this current level, the choice between synchronous rectification or an external diode will depend on the cost and circuit complexity implications.

Chapter 5 Split supply JFET driver

5.1 Introduction

In section 4.3.2, the SJEP120R125 was found to perform well in synchronous rectification applications, however, undesirable shoot through conditions were observed during rapidly falling bridge voltages. These occurred because the gate-source voltage was not being successfully maintained at zero volts. This is partially because the inductance and resistance in the gate drive circuits allows some of the drain-gate current to charge the gate-source capacitance instead of being shunted by the driver circuitry.

The problems are not necessarily confined to SiC JFETs. In [112], it was noted that the sensitivity of silicon MOSFETs has increased to enable direct driving from 5V or 3.3V logic signals and, as a consequence, this has lead to problems in some bridge configurations where rapid voltage swings cause the MOSFETs to turn on spuriously.

To mitigate the false turn-on problems, a split driver arrangement is proposed that applies a negative potential across the gate-source junction of the transistor when it is required to be off. This potential increases the spurious voltage required to turn a transistor on at an inappropriate time, improving immunity to spurious operation.

At the time of the design, the datasheet for the SJEP120R125 (revision 1.4, September 2008) also advocated the use of bipolar gate drive circuits as a cure for this problem. Bipolar gate drives were also used to prevent shoot-through in bridge circuits constructed from IGBTs in [113], with a high side negative supply derived from a chain of zener diodes across the DC bus. In this chapter, a circuit is presented as an example implementation of a bipolar JFET driver. The circuit has the novelty of combining a capacitor charge pump with a bootstrap to create a high-side and low-side bipolar gate driver capable of running from one single-ended power source. The circuit is deliberately made up of the same building blocks found in commercially available MOSFET driver ICs, to specifically illustrate the potential for a single IC solution. A single IC solution for driving a pair of normally-off SiC JFETs in a bridge from one single-ended supply is potentially very attractive to industry. Such an IC would enable existing silicon MOSFET

based power converters to be easily adapted to use normally-off SiC JFETs without redesigning their auxiliary "housekeeping" supplies which in many cases are single-ended.

Although an AC coupled output is used in this chapter, a two-stage DC coupled output similar to that published in [104] could be used instead, while still enjoying the benefits of only requiring one single-ended power supply for both JFETs.

In May 2011, CISSOID announced the commercial availability of the CHT-ATLAS[114], a dual transistor driver IC designed for use with both normally-on and normally-off SiC JFETs. The CHT-ATLAS is evidence of the commercial feasibility behind a normally-off SiC JFET driver IC. In May 2012, CISSOID followed up the CHT-ATLAS with an application note describing the use of the CHT-ATLAS in combination with CISSOID's CHT-THEMIS controller to drive normally-off SiC JFETs from Semisouth.

5.2 Design Considerations

5.2.1 Topology

The proposed driver topology, shown in Figure 5-1 is sufficiently similar to existing MOSFET driver circuits, so that much of the prototype is constructed around a standard MOSFET driver IC. Q1 and Q2 form a standard bridge leg which is to be configured as a boost converter due to the limited output voltage capability of the available power supplies. Q2 performs the function of boost switch, while Q1 provides synchronous rectification with a boost ratio of 50% to give an even share current between Q1 and Q2. A split supply of +/-7V was chosen as the +7V supply provides sufficient voltage drop across the gate impedance network to allow flexibility in the gate current characteristic without excessive losses, the -7V supply provides some shoot-through immunity and the combined 14V is within the 16V rating of many MOSFET driver ICs. R15 and R19 were chosen to limit the continuous gate current to chosen value of approximately 80mA, based on the characteristic curves in the SJEP120R125 datasheet.[Appendix C]. Assuming a 3V gate-source voltage drop for Q1 and Q2, C28 and C29 see a 11V swing. Values of 2.2nF were chosen to produce a charge transfer of 24.2nC, closely matching the 25nC gate charge of Q1 and Q2.

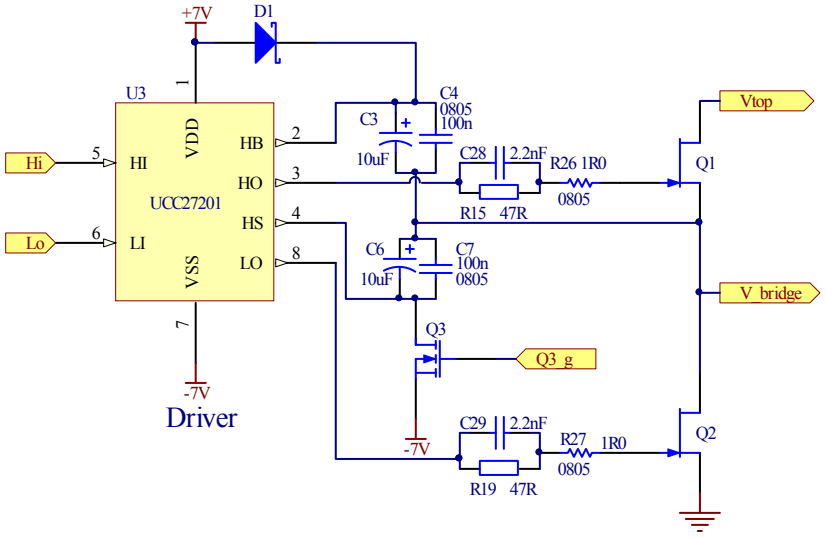


Figure 5-1: The half-bridge is driven by a standard MOSFET driver, with a split supply to ensure that the JFETs remain turned off properly when required.

U3, a UCC27201 MOSFET driver IC is configured in a standard half bridge arrangement, with boost diode D1 providing a floating supply across C3 and C4 that is charged via Q2 when Q2 is on. The design differs, however, in that the HS terminal of U3 is not connected to the source of Q1. Instead, the potential at HS is maintained at a level that is negative with respect to Q1's source as long as C6 and C7 remain charged. This causes a negative voltage to appear across the gate-source junction of Q1 when the HI input of U3 is low. By applying this negative potential, capacitor C28 is only relied upon to achieve quick turn-on and turn-off transitions and is not required for its charge pump effect. This removes the minimum capacitance constraint that would otherwise apply to C28 to ensure that it fully discharges during the off time. The practical maximum duty cycle is increased as a result, constrained only by the requirements for the bootstrap capacitors to receive sufficient charging time. Because both the positive bootstrap supply (energy stored in C3 and C4) and the negative bootstrap (energy stored in C6 and C7) can only be charged when Q2 is on and Q2's driver does not operate from a floating supply, the prototype imposes no minimum duty cycle constraint.

The positive bootstrap supply charges through D1 and Q2, analogous to classic high side MOSFET driver supply circuits. The charging of the negative bootstrap supply is unique to the proposed topology and is facilitated by a third transistor Q3. The device used for Q3 does not carry significant current but must block the full VCC potential.

5.2.2 Logic circuitry

Unlike the positive bootstrap supply, the negative supply can be overcharged if Q3 is turned on when there is a large voltage present on the bridge. To ensure that this does not occur, a control circuit is proposed in Figure 5-2 for Q3. The circuit provides an inverted PWM signal labelled LS as its input relative to the -7V logic ground and utilizes a comparator to ensure that Q3 can never be on when V_bridge is greater than 1 volt, regardless of the state of LS.

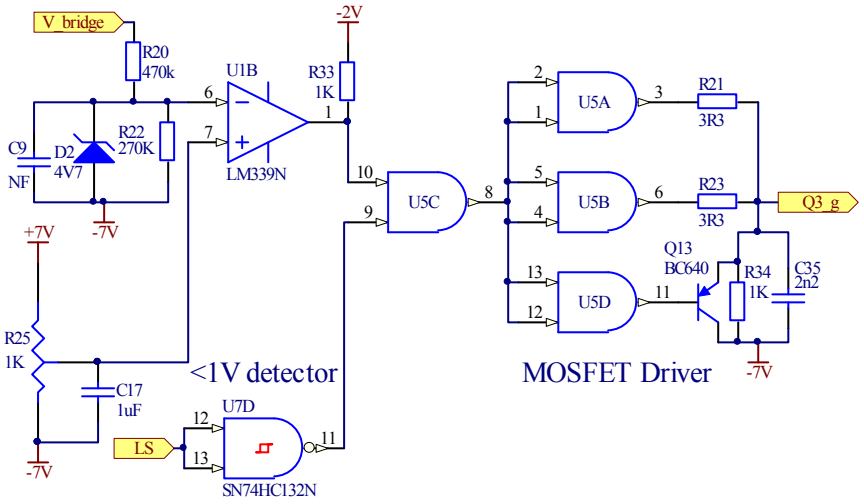


Figure 5-2: Comparator U1B prevents Q3 from turning on when V_bridge is more than 1V

R20 and R22 divide V_bridge by a factor of three. The resultant voltage is compared by comparator U1B to a reference voltage determined by R25. Because the bridge voltage can rise as high as VCC which, in many applications could be hundreds of volts, zener diode D2 clamps U1B's input, ensuring that it remains at a safe level. U1 is operated from a +/- 7V split supply and its −7V rail is common with the logic ground. Therefore, the positive logic power node is −2V relative to system ground.

Figure 5-3 shows the proposed pulse-shaping logic circuit to create the high and low side JFETs' logic signals from the same -7V referenced, inverted PWM signal applied to the Q3 logic circuitry.

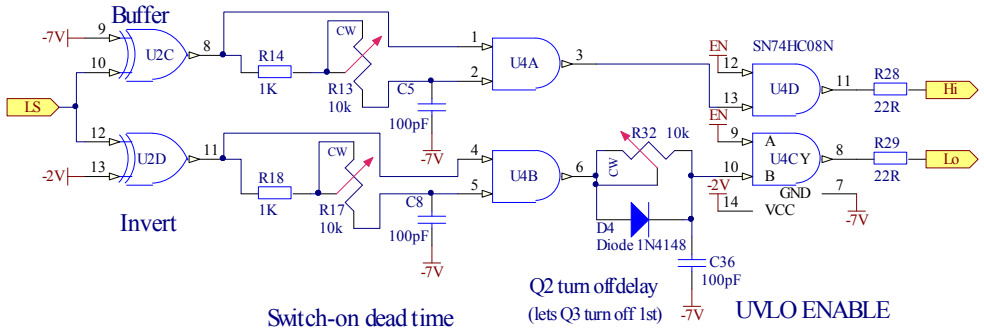


Figure 5-3: Logic circuits and delays create buffered and inverted signals as required with controllable dead time.

The logic circuit creates turn-on delays for both Q1 and Q2, allowing the dead time to be adjusted for optimum switching performance. A turn-off delay is also created for Q2 to ensure that Q3 has time to fully turn off first. The circuit uses more logic gates than the simplest logical equivalent to ensure that the propagation delays between the high and low drive signals are matched. Figure 5-4 shows an illustration of the timing for the Lo and Hi signals when the LS input is driven by a 100kHz square wave with the delays exaggerated.

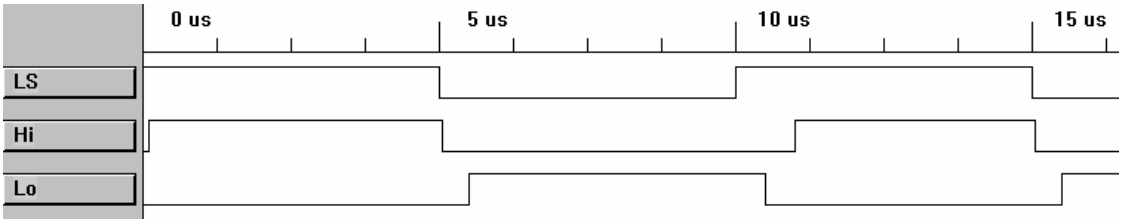


Figure 5-4: Timing diagram for the logic circuits shown in Figure 5-3 with exaggerated delays.

In the prototype circuit, the delays were adjusted by hand, while monitoring the current waveform with an oscilloscope for evidence of shoot-through. Some commercial MOSFET driver ICs offer a similar feature where the dead time between the low and high side outputs can be adjusted externally.

The high and low side JFET logic circuitry in Figure 5-3 as well as the Q3 logic circuitry in Figure 5-2 both require an inverted PWM signal referenced to −7V for correct operation. This is achieved by level-shifting a standard ground referenced TTL PWM signal using the inverting transistor network in Figure 5-5. The PWM signal, generated externally by a PWM IC or signal generator is connected to P1 and undergoes three inversions by Q6, Q4 and Q5, resulting in an inverted 5V peak to peak PWM signal that is referenced to -7V.

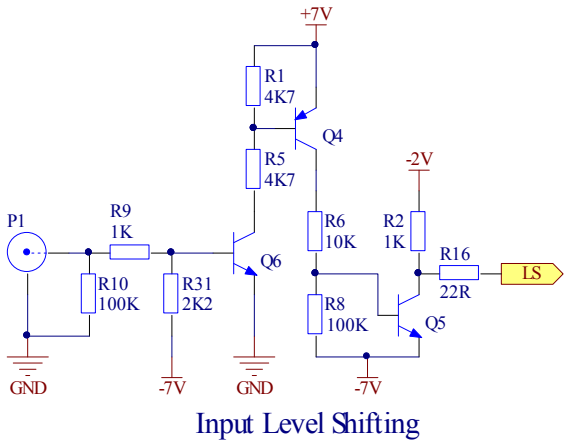


Figure 5-5: A TTL PWM signal is level-shifted down to the −7V rail

5.2.3 Applicability and Manufacturability

Manufacturability is a key priority for the JFET driver circuit which would ideally be built into a single integrated circuit. Therefore, the design choices for a prototype are limited to technologies commonly found in existing MOSFET gate driver ICs. The building blocks identified as being commonplace in MOSFET driver ICs include level-shifters, delays, logic gates, Schmitt triggers, fast diodes and comparators.

The proposed driver circuit requires a split supply that is not normally required by existing MOSFET driver ICs. To maximize ease of adoption, the prototype includes a capacitor charge pump circuit to create the negative voltage rail from the positive rail. This allows the circuit to operate from a single-ended external supply as shown in Figure 5-6.

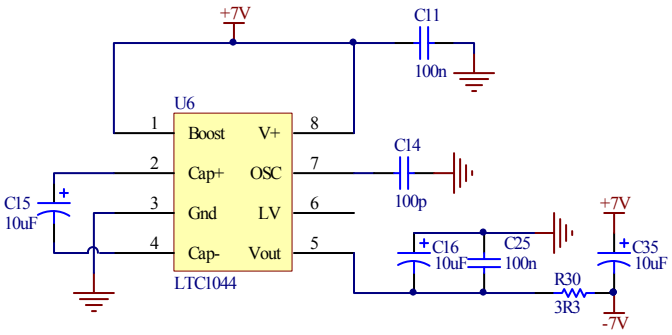


Figure 5-6: The charge pump circuit generates a negative supply rail

U6, a LTC1044 charge pump controller uses C15 to create a negative supply rail by inverting the positive supply. C14 sets the charge pump oscillator frequency to approximately 23kHz, slightly above the human audible range.

5.2.4 -7V rail power consumption

The power consumption from the −7V rail must be calculated to ensure that C15 is large enough to prevent excessive voltage ripple from occurring.

When one of the JFETs is on, its gate-source voltage is approximately 3V, based on gate characteristics and current limiting resistor values. The energy required to swing its gate-source voltage to −7V is calculated in *Eq 5-1*.

$$\begin{aligned} E &= \frac{1}{2}CV_{before}{}^2 + \frac{1}{2}CV_{after}{}^2 \\ &= \frac{1}{2}C(V_{before}{}^2 + V_{after}{}^2) \\ &= \frac{1}{2}\cdot 610\times 10^{-12}\cdot\left(3^2+(-7)^2\right) \\ &= 17.7nJ \end{aligned} \qquad \textit{Eq 5-1}$$

At a switching frequency of 100kHz, the two JFETs combined will consume 3.5mW from the −7V rail.

Because the capacitance of Q3 is likely to be similar to the JFETs', the amount of power drawn from the −7V rail to turn off Q3 is assumed to be 1.75mW. The four 74HC series logic gate packages each have a quiescent current rating of 6-20µA resulting in a total of, at most, 0.6mW.

The UCC27201 has a significantly larger quiescent current of 0.4mA or 2.8mW from the −7V rail. This gives a total worst case estimate of overall power draw from the −7V rail of 8.6mW. At 23kHz, the energy transferred during each charge pump cycle would need to be at least 374nJ. The ripple voltage is calculated in *Eq 5-2*.

$$\begin{aligned} \Delta E &= \frac{1}{2}C\left(V_{\max}{}^2 - V_{\min}{}^2\right) \\ 374nJ &= \frac{1}{2}\cdot 100\times 10^{-9}(7^2 - V_{\min}{}^2) \\ V_{\min} &= 6.44V \\ V_{ripple(pk-pk)} &= 556mV \end{aligned} \qquad \textit{Eq 5-2}$$

A voltage ripple of 556mV is acceptable for this application because the DC-DC converter stages used in Eaton's telecommunications power supplies have sufficient input noise rejection to tolerate up to $1V_{pk}$ of ripple on this input without exceeding their maximum output noise specifications. Therefore, the capacitance of C15 and the switching frequency are an appropriate combination.

5.3 Prototype JFET driver circuit

A prototype JFET driver circuit was designed by merging together the sub-circuits in Figure 5-1, Figure 5-2, Figure 5-3, Figure 5-6 and Figure 5-5 and adding appropriate decoupling capacitors and ancillary power supply components. The combined schematic appears in Appendix B, Schematic 3.

SJEP120R125 SiC JFETs are used for Q1 and Q2, while a 600V Infineon Technologies (Infineon) IPP60R125CP MOSFET is used for Q3. The choice of transistor for Q3 has a negligible effect on circuit performance because it carries an extremely small current, though the device used in this prototype limits the maximum V_{cc} voltage to 600V.

Figure 5-7 shows the PCB layout, created for the proposed prototype JFET driver circuit, with its ground planes hidden for clarity. Q1, Q2, Q3 and D1 are placed particularly close together and MOSFET driver U3 is located on the bottom layer to achieve close proximity to these devices. The layout implements good design practices and minimizes the loop area of load current paths by keeping power circuitry densely populated in the top right corner of the PCB.

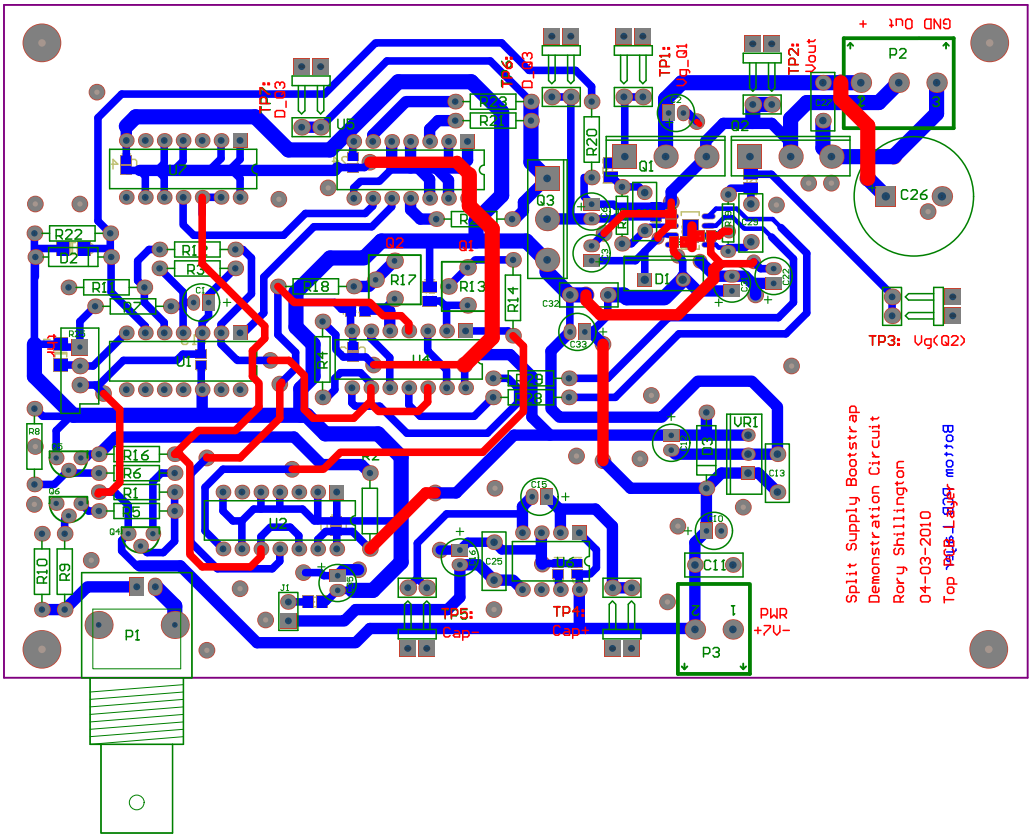


Figure 5-7: PCB layout for the proposed prototype driver ciruit (ground planes hidden for clarity)

An external PWM source is applied via connector P1, while the single ended 7V power supply is connected to P3. P2 connects the high voltage source and load to the PCB. Special wire loops are provided for test points TP1, TP2 and TP3 to allow the connection of oscilloscope probes with minimal stray inductance.

5.3.1 Construction of the prototype driver circuit

The prototype driver circuit was constructed on a double-sided circuit board shown in Figure 5-8, etched from the pattern in Figure 5-7.

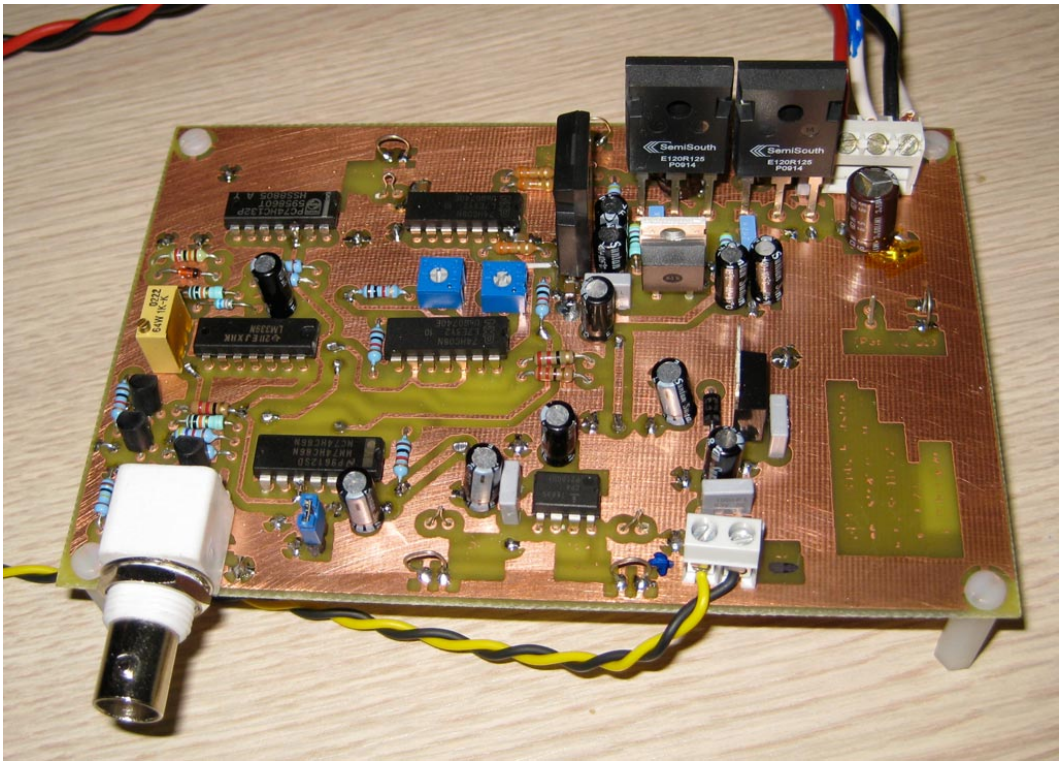


Figure 5-8: The dual bootstrap JFET driver prototype, constructed from a mixture of semiconductor building blocks typically found in MOSFET driving ASICs and common passive components

5.3.2 Performance of the prototype driver circuit

With the addition of an external voltage source, inductor and load, the prototype driver circuit was used to create a boost converter as shown in Figure 5-9.

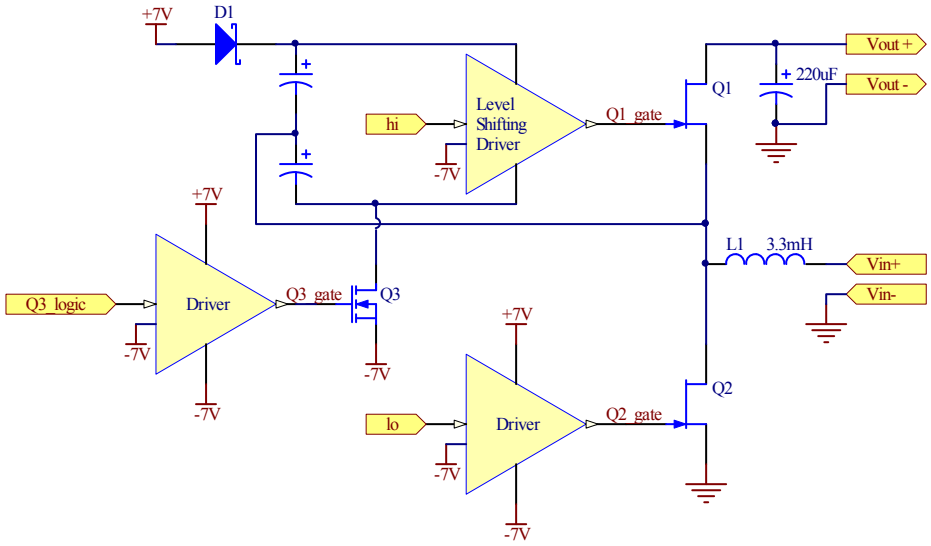


Figure 5-9: Gate driver configured as a boost converter

The logic signals observed in the driver circuit are shown in Figure 5-10, relative to the circuit ground, i.e. -7V being logic low and -2V being logic high. Due to diode voltage

drops in the capacitor charge pump, the -7V rail was approximately -5V in practice, resulting in approximately -5V for a logic low and 0V for a logic high. A small dead time can be observed between the high and low side transistors' logic signals, ensuring that shoot-through conditions do not occur. A large dead time can be seen between the low-side logic transitioning high and Q3's logic transitioning high. This allows time for the bridge voltage (appearing across the low-side transistor's channel) to fall to a sufficiently low level before Q3 turns on. Q3's logic pre-emptively transitions low before the low-side transistor does. These dead times around Q3 prevent the full load voltage from being applied across the high-side bootstrap capacitors.

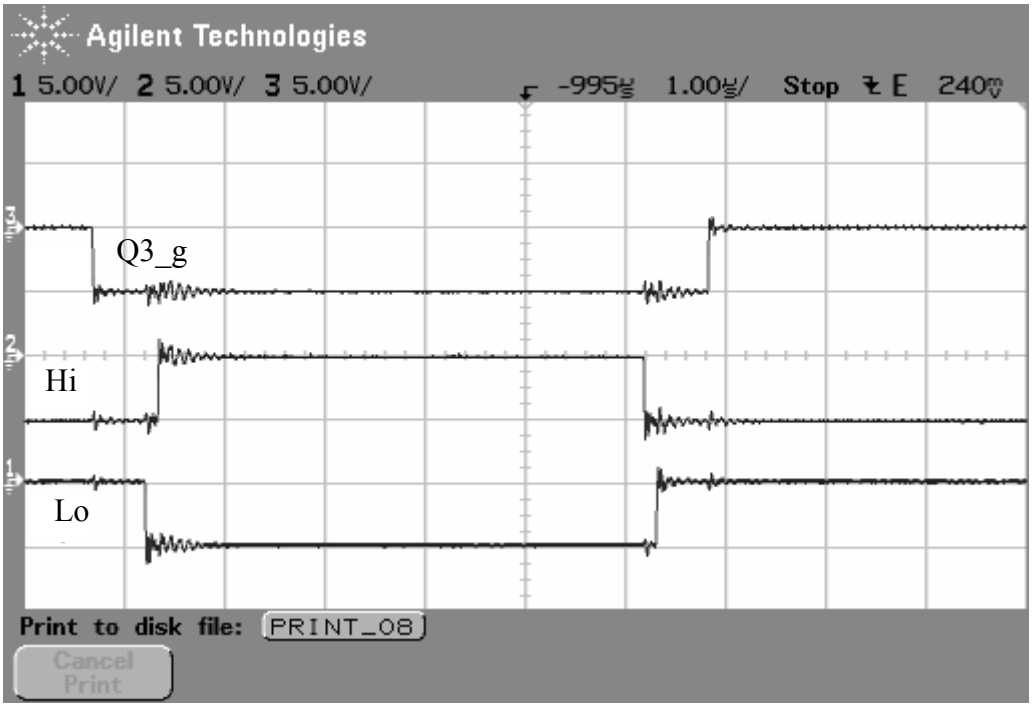


Figure 5-10: Logic signals for the high-side transistor Q1 (middle trace), low-side transistor Q2 (lower trace) and Q3 (upper trace)

Figure 5-11 shows the gate-source voltages of Q1 and Q2 as well as the gate voltage of Q3 while boosting 60V to 120V at a power level of 180W. The gate-source voltages of both Q1 (middle trace) and Q2 (top trace) can be seen swinging well below ground at turn-off (Vgs_{Q1} was measured differentially using the oscilloscope's mathematics facility and is shown with the horizontal axis as the zero volt reference and 5 volts per division). After Q2 turns off and the dead time has elapsed, Q1 turns on. The rising bridge voltage causes current to flow through Q2's drain-source capacitance, resulting in a visible voltage spike on Q2's gate. The spike remains well below ground and no shoot-though occurs. Similarly,

when Q2 turns on, a spike is visible on Q1's gate-source voltage. This spike is larger than that on Q2 but is still not sufficient to cause a shoot-through condition.

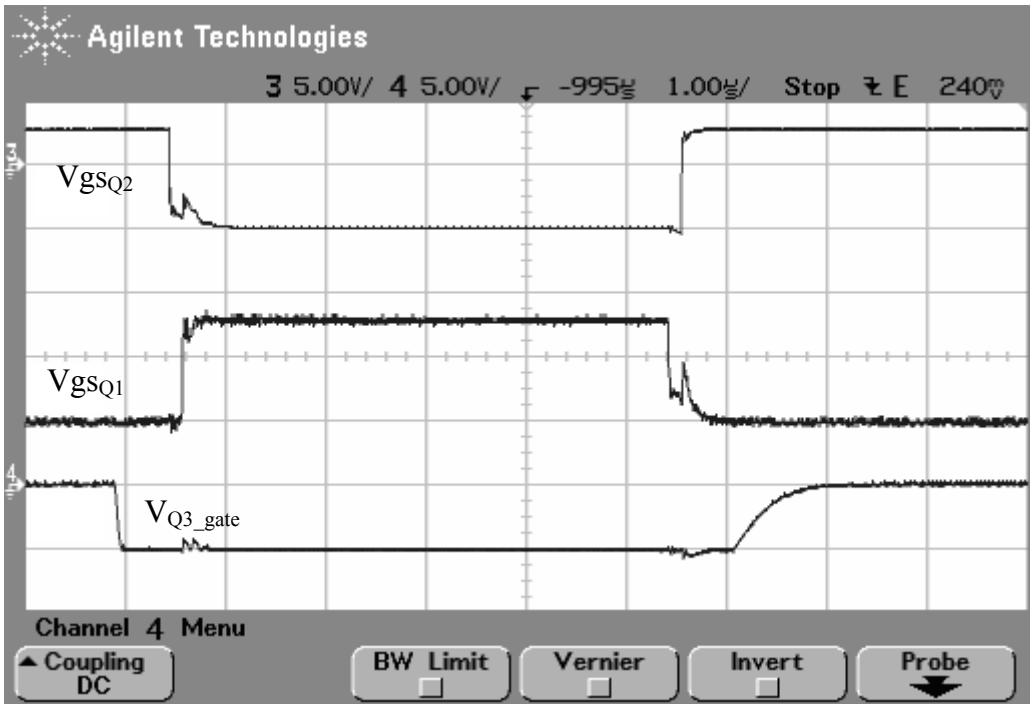


Figure 5-11: Basic operation showing Vgs_{Q1} (middle), Vgs_{Q2} (top) and V_{Q3_gate} (bottom, relative to circuit ground, not Q3's source). Vgs_{Q1} is shown with zero at the central horizontal axis (immediately above the "Vgs_{Q1}" label) and has a scale of 5V/div.

The spikes observed in Figure 5-11 as a result of capacitive coupling between the drain and gate of Q1 are not large enough to cause false turn-on and are expected to be significantly smaller when the circuit is combined into an integrated circuit. Therefore, the negative gate voltage applied to Q1 during Q1's off time provides sufficient margin to prevent shoot-through from occurring on the bridge at the conditions tested. If larger dv/dt rates are achieved due to a faster turn-on of Q2 than occurred in the test in Figure 5-11, the negative supply rail could be increased (by increasing the voltage supplied to the capacitor charge pump).

A number of methods in the literature could also be considered for mitigating spurious turn-on problems. In [115], a reduction in the dv/dt of the bridge was shown to work well with silicon MOSFETs, though this could results in increased switching losses. Another possibility is to add small capacitors across the gate and source terminals of each JFET to improve the gate-source to gate-drain capacitance ratio, allowing more of the drain-gate current to be shunted to the source. Since the conclusion of the research presented in this

thesis, it was shown in [116] that the addition of such capacitors does not significantly decrease switching speed. It was further suggested in [116] that RC snubbers could be used across the DC bus as well as separate heatsinks for Q1 and Q2 to minimise capacitive coupling. The use of a negative gate-source voltage at turn-off as in the author's driver circuit was also advocated in [116]. In [117], shoot-through was inherently protected against by the insertion of a diode in series with Q2's drain and connection of Q1's gate to the diode's cathode. This approach is not suitable for the topology proposed here because current needs to flow in both directions through Q2.

To test the gate driver at very high duty cycles without very large output voltages, the input and output connections of the circuit in Figure 5-9 were reversed, creating a buck converter. The buck converter was then operated with a 95% duty cycle PWM signal at a switching frequency of 100kHz. The voltage across bootstrap capacitors C3 and C4 was measured and although significant voltage ripple of approximately $1V_{pk\text{-}pk}$ was observed (as expected), the voltage always remained above 5V. 5V is sufficient with the chosen value of R15 to ensure that sufficient gate current flows through Q1 to maintain a conducting state for the entirety of the 9.5µs on time.

5.3.3 Context of Semisouth Driver

Soon after the construction of the prototype driver circuit presented in this chapter, SemiSouth published an application note [104] advocating the use of a two-stage bipolar driver to achieve faster switching transitions. The driver proposed by Semisouth uses logic circuitry to generate short pulses that are used to briefly turn on a very low impedance gate drive in parallel to a larger impedance gate drive that maintains the turned-on state of the JFET for the duration of the PWM on-time. This arrangement should achieve very good switching speeds. However, the design presented by Semisouth requires an external split rail power source that does not satisfy the easy adoption criterion. The unique features of both designs could conceivably be combined into an even better solution. Specifically, the Semisouth driver features an output stage for delivering large pulses of current at turn-on and turn off as well as a second, separate output stage for delivering sustained gate current during the conducting state. This could be combined with the feature of a self-contained charge-pump based negative supply rail that was used in the driver proposed in this chapter.

5.4 Conclusions

The proposed JFET driver circuit alleviates the shoot-through problems that were experienced in section 4.3.2 by applying a low impedance negative gate-source potential to the SiC JFET at turn-off. The use of typical MOSFET driver IC building blocks in the gate drive circuit presented in this chapter supports the notion that a single chip version is a practical possibility. Extending the proposed normally-off SiC JFET driver circuit to utilize separate pulse and sustained current drives for the JFET instead of a paralleled resistor-capacitor network could potentially improve the attainable switching speeds, increasing the attractiveness of the driver.

Chapter 6 High Efficiency PFC Circuit

6.1 Introduction

A particular single-phase 2kW telecommunications rectifier application requires a switching frequency of at least 100kHz in order to reasonably be expected to meet strict EMI, distortion, control loop bandwidth, electrical efficiency and physical size requirements. These requirements generally become easier to meet as switching frequency increases, however switching frequencies much above 200kHz can worsen EMI due to low order harmonics of the switching frequency occurring at higher frequencies where emissions limits are tighter. Excessively high switching frequencies also cause unacceptably high switching losses that preclude meeting the very high electrical efficiency targets (98% peak efficiency).

Although old, the power factor correction PFC circuit topology presented in [118] has been identified as a topology worth reconsidering in light of the new characteristics of the SiC JFET. The topology is attractive because current only flows through one semiconductor device at any time, resulting in reduced conduction losses compared to other topologies which contain two or three semiconductors in series with current flow. With 900V silicon MOSFETs, the PFC topology of interest is unable to adequately meet the minimum switching frequency (100kHz) for the telecommunications rectifier application due to the 900V MOSFETs' poor switching speeds leading to excessive switching losses. 600V silicon MOSFETs are also unable to be used in this topology due to their inadequate voltage rating. Normally-off SiC JFETs appear to enable the use of this topology at switching frequencies in excess of 100kHz because of their high blocking voltage and rapid switching speed. The reduced conduction losses of this topology could allow for a power factor correction circuit with exceptionally high efficiency to be developed which is of significant commercial interest. For commercial and practical reasons, it is preferable that a normally-off SiC JFET based PFC circuit utilize the same 120µH boost inductor employed in existing telecommunications rectifier designs because its electrical losses and cost have already been carefully minimised without compromising on manufacturability. As such, investigations were restricted to use of this particular inductor.

A DC equivalent of the PFC topology of interest is used extensively in this chapter to model the instantaneous operating conditions of the AC PFC circuit at a particular point in the AC mains cycle. By calculating these conditions at enough discrete points spaced equally in time over a mains quarter-cycle, their average is used to model the steady-state AC performance of the PFC. 0 describes the design of a prototype DC equivalent circuit to test the mathematical model from Chapter 6. The measured results are then presented in Chapter 8 over a subset of the modelled operating range, limited by shortcomings of the prototype's control circuitry.

6.2 Circuit Operation

6.2.1 Overview

The PFC topology is shown in its simplest form in Figure 6-1. The circuit consists of a half bridge or inverter leg connected in reverse to achieve rectification. The circuit behaves analogously to a standard boost converter with transistors Q1 & Q2 (and their anti-parallel diodes) alternating between being the PWM switch and the rectifier depending on the instantaneous polarity of the mains. Synchronous rectification is performed to minimize conduction losses with the anti-parallel SiC Schottky diodes conducting during the dead times between Q1 and Q2 conducting. Like a standard PFC boost converter, the output voltage must be larger than the input voltage. With a nominal 230V RMS input, the minimum voltage across each of C1 and C2 is 325V. Q1 and Q2 must be able to block twice this voltage, precluding the use of 600V devices. A PWM control implementation for this topology was proposed in [119].

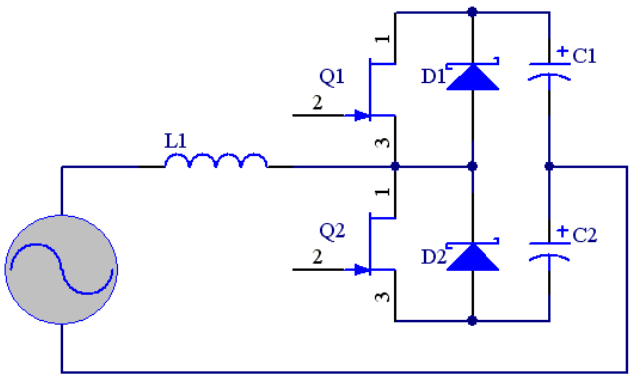


Figure 6-1: High Efficiency PFC topology

During any positive mains half-cycle, the circuit is equivalent to that shown in Figure 6-2. During negative half cycles, by symmetry, the circuit is similar, except that Q1 & Q2 exchange roles as do C1 and C2. If C2 were removed, the DC equivalent circuit is analogous to a classic boost converter.

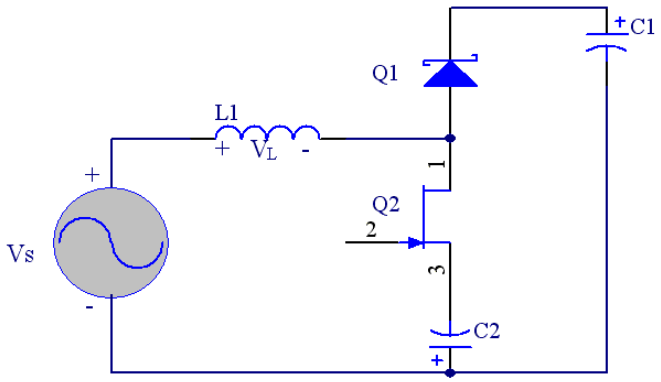


Figure 6-2: Equivalent circuit during a positive mains half-cycle

In many power factor correction boost circuits, the DC output voltage is typically 400V (requiring the use of transistors that can block substantially more than 800V). The input is typically supplied from an AC utility for example the 230V RMS, 50Hz voltage v_s in *Eq 6-3*.

$$v_S = 325 \cdot \sin(100 \cdot \pi \cdot t) \qquad \textit{Eq 6-3}$$

The exact magnitude of the output voltage is a design decision that balances the capacitor breakdown voltage against energy storage and varies from one manufacturer to another. The value used does not affect the overall operation, provided it meets the criterion of being greater than the peak of v_s. By varying the duty cycle of Q2, the average current through v_s and L1 can be kept directly proportional to v_s, resulting in a power factor close to unity. With input filtering, the input current PFC operating at 2kW from a 50Hz 230V RMS supply is defined in *Eq 6-4*.

$$i_S = v_s \cdot \frac{I_{pk}}{V_{pk}}$$

$$= 230 \cdot \sqrt{2} \cdot \sin(100 \cdot \pi \cdot t) \cdot \frac{\left(\frac{2000}{230}\right) \cdot \sqrt{2}}{230 \cdot \sqrt{2}} \qquad \textit{Eq 6-4}$$

$$= \frac{2000}{230} \cdot \sqrt{2} \cdot \sin(100 \cdot \pi \cdot t)$$

The input current is slowly scaled by using a much slower outer control loop to maintain the correct output voltage as the load changes.

6.2.2 Boost operation

The DC equivalent circuit can operate in either continuous conduction mode, critical conduction mode or discontinuous conduction mode. An illustration of typical inductor current waveforms for each of these modes is shown in Figure 6-3. The slopes of the waveform and the particular mode that occurs at any particular operating point depend on the input voltage, output voltage, load, switching frequency and inductance. A switching frequency of 100kHz and inductance of 120µH were used in the illustration, with the other circuit values chosen arbitrarily.

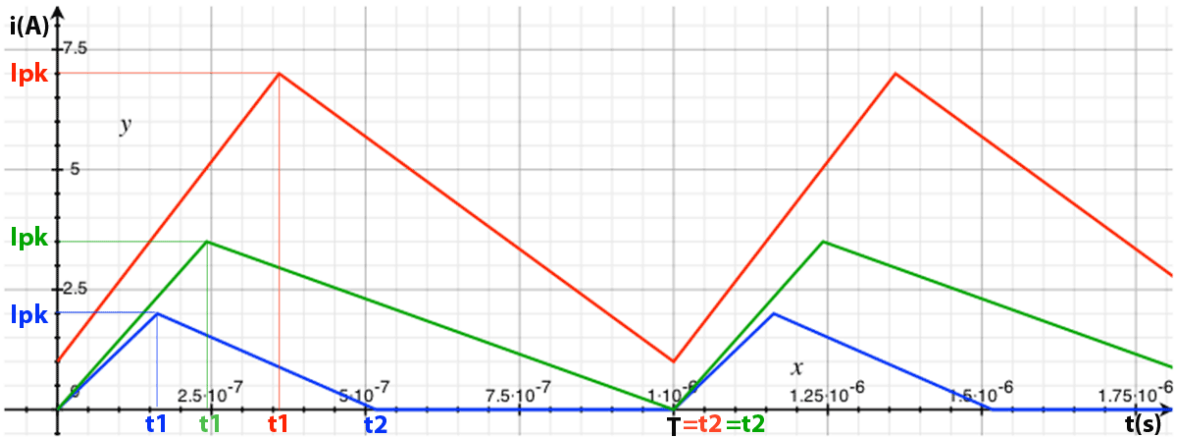


Figure 6-3: Illustration of the inductor current waveform against time in continuous conduction mode (red), critical conduction mode (green) and discontinuous conduction mode (blue)

Referring to Figure 6-2 when switch Q2 is on, the voltage applied across inductor L1 is the sum of V_S and V_{C2}. When Q2 is off, V_L is the difference between V_{C1} and V_S. Assuming a short term average of approximately zero volt-seconds appears across L1, equality in *Eq 6-*

5 can be written, where *D* is the duty cycle of Q2, T is the switching period and the circuit is operating in either continuous or critical conduction mode.

$$D \cdot T \cdot (V_S + V_{C2}) = (1 - D) \cdot T \cdot (V_{C1} - V_S) \qquad \textit{Eq 6-5}$$

Eq 6-5 can then be rearranged to the form in *Eq 6-6*.

$$\frac{V_{C1} - V_S}{V_S + V_{C2}} = \frac{D}{1 - D} \qquad \textit{Eq 6-6}$$

C2 would normally be a short circuit in a classic boost converter, so setting V_{C2} equal to zero in *Eq 6-6* results in the classic boost converter relationship as shown in *Eq 6-7* where *Vs* is the input voltage and V_{C1} is the output voltage.

$$\begin{aligned} \frac{V_{C1} - V_S}{V_S + 0} &= \frac{D}{1 - D} \\ \frac{V_{C1}}{V_S} - 1 &= \frac{D}{1 - D} \\ \frac{V_{C1}}{V_S} &= \frac{D + (1 - D)}{1 - D} \\ \frac{V_{C1}}{V_S} &= \frac{1}{1 - D} \end{aligned} \qquad \textit{Eq 6-7}$$

In *Eq 6-8*, the relationship from *Eq 6-6* has been rearranged to make *D* the subject, allowing the duty cycle of the boost converter to be calculated at any operating point.

$$D = 1 - \frac{1}{\left(\frac{V_{C1} - V_S}{V_S + V_{C2}} + 1\right)} \qquad \textit{Eq 6-8}$$

Figure 6-4 illustrates the duty cycle that is required to achieve a 400V DC output across C1 over the input voltage range for a variety of voltages across capacitor C2 in critical or continuous conduction mode. A 30V droop in V_{C2} to 370V does not cause a significant change in duty cycle and the circuit is able to continue boosting near zero crossings (V_S=0) with less than 100V remaining across C2, without an unreasonably high duty cycle.

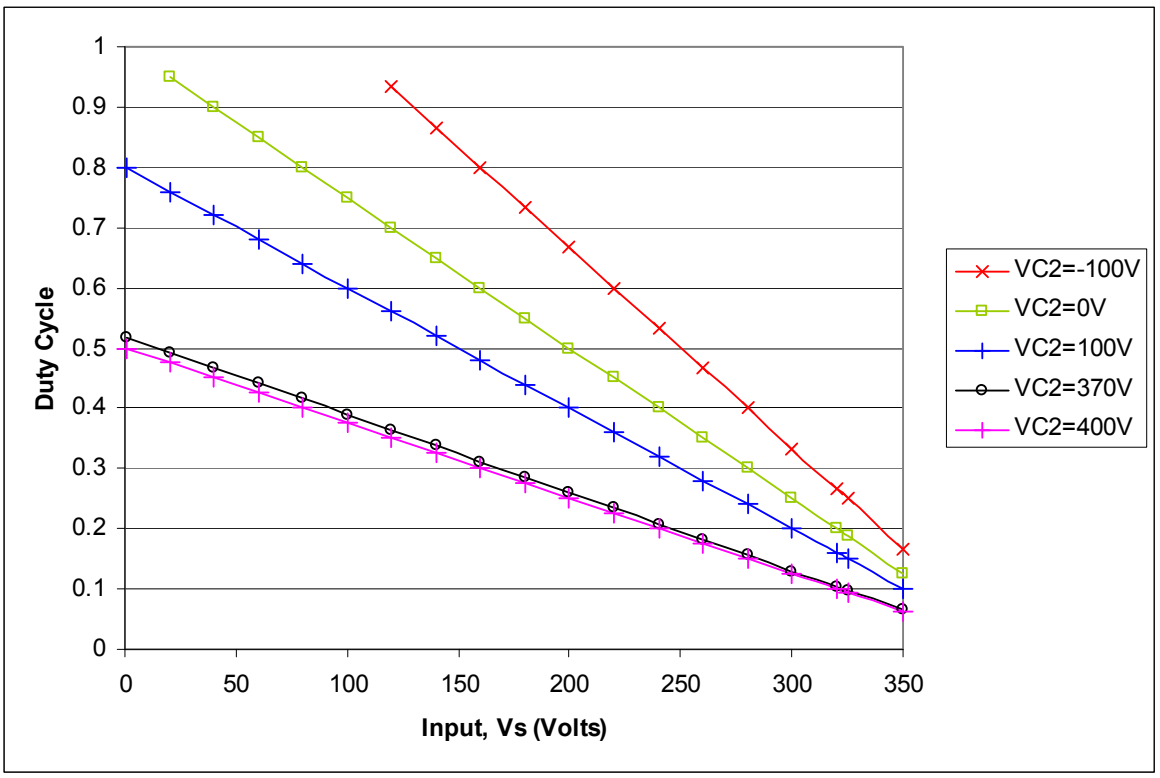


Figure 6-4: Duty cycle required to achieve a 400V output from a range of input voltages (V_S) at a variety of values of V_{C2}.

It is even theoretically possible for this topology to operate with a negative voltage for V_{C2}, (provided Vs is greater in magnitude than V_{C2}), but such an operating point is impractical, particularly because of the need for a large amount of non-polarized capacitance. The observation does demonstrate that circuit operation is not impeded by voltage ripple across C2 and that capacitors should, therefore, be chosen to achieve voltage ripple goals related to the load's requirements. For the purposes of the remaining analysis throughout the thesis, it will be assumed that the voltages across C1 and C2 remain equal with the understanding that ripple can be compensated for by a change in duty cycle.

6.2.3 Discontinuous Conduction Mode

As a mains zero crossing is approached, the average current through the boost inductor tends to zero and the converter goes into discontinuous conduction mode at a point defined by load, switching frequency and inductance. Some flexibility exists in the placement of the continuous/discontinuous boundary by adjusting the boost inductor's value, but these are limited by the need for a practical PFC circuit to be able to react to sudden changes in

loading. The additional restriction here is the required use of a specific 120μH inductor (as identified at the start of Chapter 6).

During discontinuous conduction, the inductor current is zero for part of each switching cycle. Like the continuous or critical conduction scenarios, the duty cycle is still controlled such that a power factor of nearly unity is achieved. The long term average inductor current remains sinusoidal over a mains cycle and can be calculated if the input power, and voltage are known. The relationship between input power and time is defined in *Eq 6-9*.

$$p_{in} = P_{in(av)} \cdot \left(1 + \sin^2(\omega t)\right) \qquad \textit{Eq 6-9}$$

When Q2 is switched on, the initial inductor current is zero and follows the relationship in *Eq 6-10* until Q2 is turned off at some time $t_1=DT$ where i_L is at its peak magnitude I_{pk}.

$$i_L = \frac{V_s + V_{C2}}{L} \cdot t \qquad \left| t_0 < t < t_1 \right. \qquad \textit{Eq 6-10}$$

The inductor current then falls from the peak value that was reached at $t=t_1$ until it reaches zero at $t=t_2$ as defined by *Eq 6-11* and illustrated in Figure 6-3.

$$i_L = I_{pk} - \frac{V_{out} - V_s}{L} \cdot (t - t_1) \qquad \left| t_1 < t < t_2 \right. \qquad \textit{Eq 6-11}$$

Time t_2 represents the time at which the inductor current reaches zero and is less than the switching period during discontinuous conduction mode. *Eq 6-11* can be written as

$$\frac{V_s + V_{C2}}{L} \cdot t_1 = \frac{V_{out} - V_s}{L} \cdot (t_2 - t_1) \qquad \textit{Eq 6-12}$$

The time at which the current through the inductor reaches zero, t_2 can be written in terms of circuit voltages, duty cycle and switching period as *Eq 6-13*, allowing t_2 to be calculated at any operating point.

$$t_2 = \frac{V_s + V_{c2}}{V_{out} - V_s} \cdot t_1 + t_1 = \left(\frac{V_s + V_{c2}}{V_{out} - V_s} + 1 \right) \cdot DT \qquad \textit{Eq 6-13}$$

Because the inductor current is zero after t_2 during discontinuous conduction mode, the average inductor current, I_{Lav} is defined by *Eq 6-14*.

$$I_{Lav} = \frac{I_{pk}}{2} \cdot \frac{t_2}{T} = \frac{(V_s + V_{C2}) \cdot t_1}{2 \cdot L} \cdot \frac{t_2}{T} \qquad \textit{Eq 6-14}$$

Eq 6-14 can be expressed as *Eq 6-15* by substituting in *Eq 6-13*. This allows the average inductor current to be calculated at any discontinuous conduction mode operating point where the circuit voltages, duty cycle and switching frequency are known.

$$I_{Lav} = \frac{(V_s + V_{C2}) \cdot DT}{2 \cdot LT} \cdot \left(\frac{V_s + V_{c2}}{V_{out} - V_s} + 1 \right) \cdot DT \qquad \textit{Eq 6-15}$$

The two *D* terms in *Eq 6-15* cause I_{Lav} to be proportional to the square of the duty cycle, as shown graphically in Figure 6-5 for a number of input voltages with the practical-restricted specific inductance of 120µH and switching frequency of 100kHz. If the duty cycle is increased beyond the end of any particular curve in Figure 6-5, the converter enters continuous conduction mode and *Eq 6-15* no longer applies.

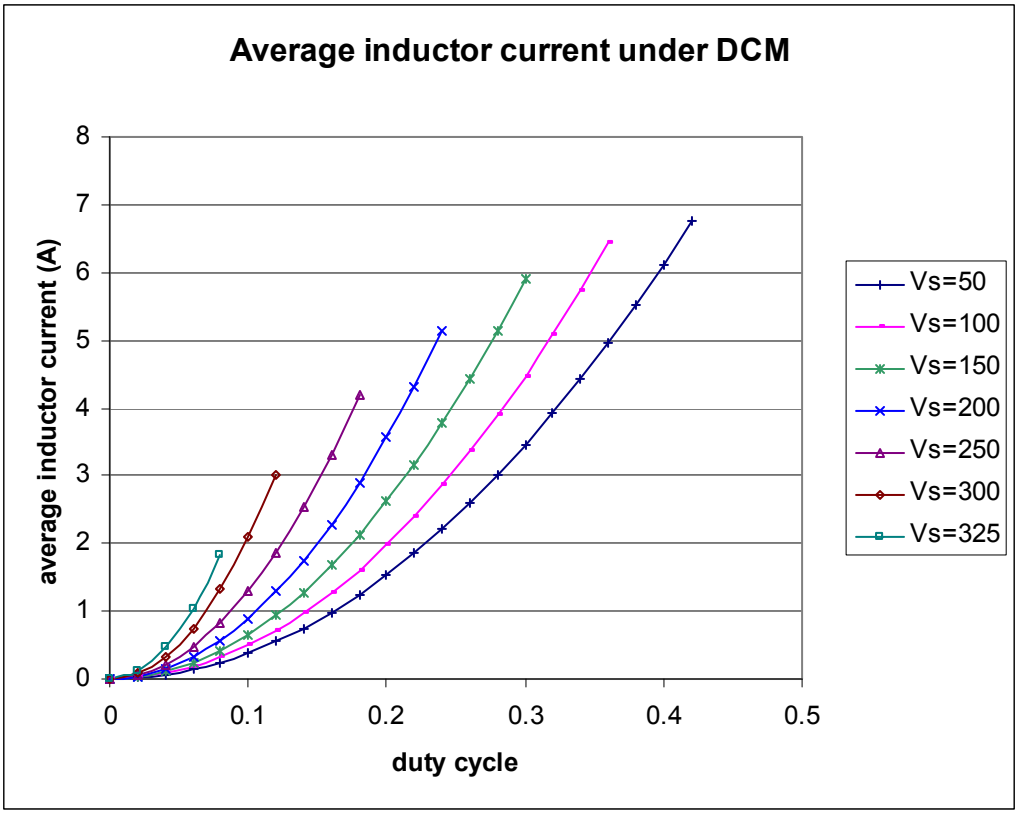


Figure 6-5: The average inductor current increases with the square of the duty cycle, and decreases with increasing supply voltage

6.2.4 Continuous Conduction Mode

If the time calculated for t_2 using the discontinuous conduction mode from *Eq 6-13* is greater than T, the switching period, the circuit is operating in continuous conduction mode. In this case, $t_2 = T$ and the $\frac{t_2}{T}$ term in *Eq 6-14* becomes equal to 1.

It is of commercial interest that a PFC circuit based on the topology in Figure 6-1 be sized at 2kW to form the front-end of a telecommunications power supply, operating from 230V AC. The operating conditions of the DC equivalent circuit in Figure 6-2 were calculated iteratively at points spaced 20V apart along a 230V RMS voltage sinusoid with $V_{C1} = V_{C2}$. Figure 6-6 shows the duty cycles that were calculated with the boundary between continuous and discontinuous conduction modes found to occur at approximately 160V.

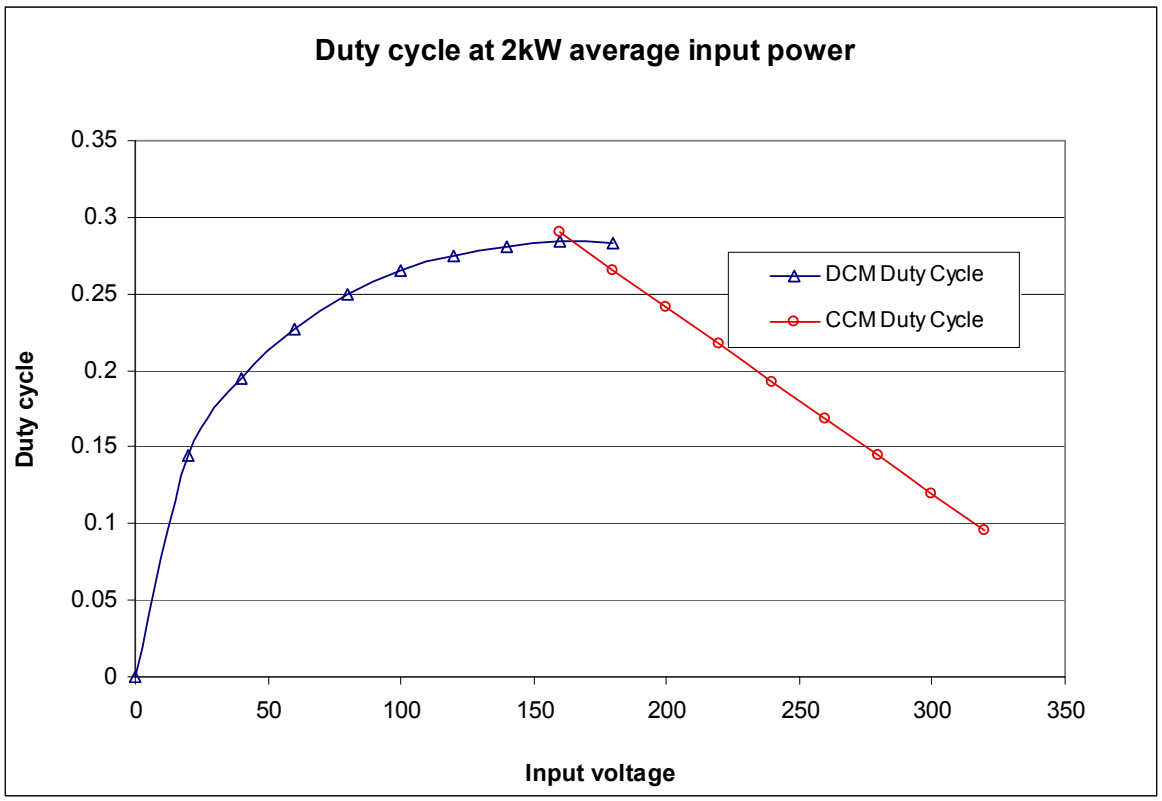


Figure 6-6: Duty cycle required to achieve a 2kW unity power factor load from a 325 volt peak sinusoidal input voltage

6.2.5 Load Configuration

In many applications, a DC-DC converter will be connected to the output of a PFC circuit to step down its DC output to a lower voltage. There exists some flexibility in the way that this DC-DC converter is connected to the split output of the PFC topology of Figure 6-1. It should be noted here that this load configuration discussion section is included to address some practical load issues given the use of the PFC topology of interest, and is not directly related to the use of SiC devices in that PFC topology.

One possibility is to utilise the centre point between C1 and C2 to allow a half-bridge to drive the DC-DC converter's transformer. This has the advantages of minimising the number of transistors in the DC-DC stage and the cancellation of some of the voltage ripple on C1 and C2. It also requires the use of transistors capable of blocking 800V DC such as 900V MOSFETs or 1200V SiC JFETs. Unfortunately imbalances can occur between the voltages across C1 and C2, though a specialized control scheme such as those in [120], [121] or [119] can solve this problem.

Another possible load configuration is to have two separate DC-DC converters, one powered from C1 and the other from C2. This allows lower voltage devices to be used and voltage imbalances to be corrected by modulating the power drawn by each converter. If the modulation is taken to the extreme, it is possible to draw full load from C1 during positive mains half-cycles and C2 during negative half-cycles. This unusual arrangement would result in the minimum the amount of energy flowing backwards and forwards between the C1 and C2. It also minimizes capacitor ripple currents (and associated losses).

While this technique is good in theory, it is wasteful and costly due to the duplication of the two complete full bridge DC-DC stages with their own transformers and four transistors each, rated for carrying the full load but only turned on half the time.

A better solution is to use the topology shown in Figure 6-7, a derivative of the asymmetrical half bridge converter [122]. The topology is well suited to this application because only four transistors and one transformer are required, yet the transistors only have to withstand the voltage of a single output rail.

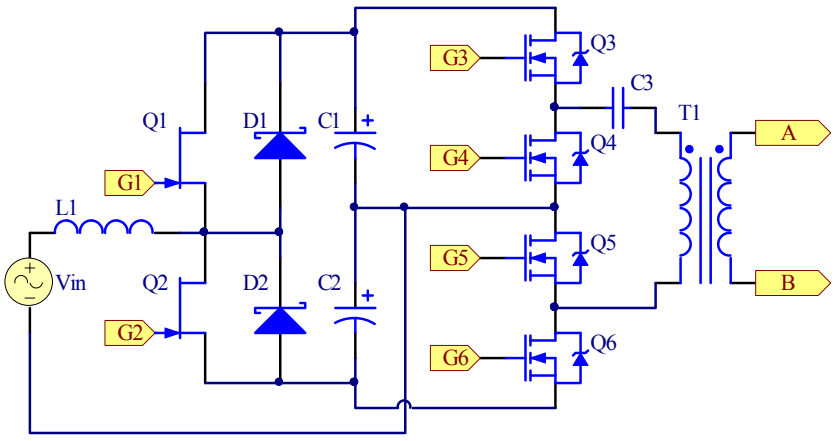


Figure 6-7: Proposed DC-DC loading arrangement

The conduction modes are shown in Figure 6-8. The converter operates by switching repeatedly through the four conduction modes in sequence. The switching pattern can also be adjusted to balance the voltages across C1 and C2. When they are similar enough, the normal pattern is used however, if C1 has a larger voltage than C2, the converter skips modes three and four. Alternatively if C2 has a larger voltage than C1, then modes one and two are skipped.

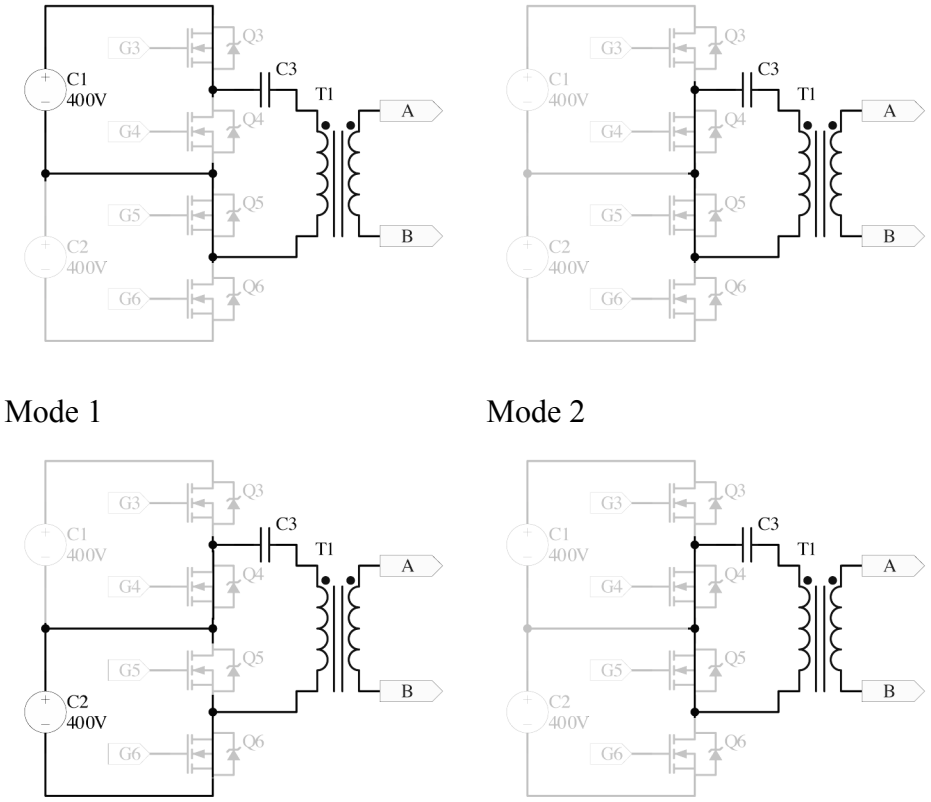


Figure 6-8: Conduction modes for the DC-DC loading configuration

In operation, the voltage appearing across the series combination of C3 and T1 alternates between 400V and 0V. The leakage inductance of T1 (or a suitably designed inductor connected in parallel) and series capacitor C3 allow operation with an asymmetrical PWM duty cycle as described in [122].

Alternatively, the load can be connected across just one of the output capacitors of the PFC and a RSCC can be used to balance the voltages across the capacitors as described in [123].

6.3 DC modelling of unique characteristics

It was shown in *Eq 6-6* that the PFC topology in Figure 6-1 has a different relationship between duty cycle and boost ratio to the classic boost converter topology. One of the key differences is because of the discharging of capacitor C2 in series with the supply V_S during positive mains half-cycles to charge capacitor C1. This results in energy transferring back and forth between C1 and C2. If voltage ripple is maintained at a sensible level, the voltage across C2 will always be greater than the input voltage V_S, resulting in

more power being drawn from C2 than V_S when Q2 is on. Although this condition appears suboptimal, the sum of V_S and C2 causes a much faster rise in inductor current than would occur in the classic boost converter, significantly reducing the duty cycle and, therefore, the time during which this condition occurs. This reduction in duty cycle was already accounted for in the calculations in section 6.2.

In the DC equivalent circuit the transient charging of C1 over a 10ms mains half-cycle cannot occur and the energy that would normally go into C1 is instead dissipated by the load. The calculations in section 6.2 deliberately relied on input power instead of output power, allowing them to remain a valid representation of the AC circuit. Because the load in the DC equivalent circuit simulates both the energy that would have been stored in C1 and that would have been supplied to the load, a direct efficiency calculation is not possible from the input and output power alone. Instead, the losses are calculated by summing the power flowing into the DC equivalent from both V_S and VC2 and subtracting the load power from this. The can then be calculated based on the losses as a proportion of input power from V_S in *Eq 6-16*.

$$\begin{aligned}\eta &= 1 - P_{loss} \\ &= 1 - \frac{P_{Vs} + P_{C2} - P_{load}}{P_{Vs}} \\ &= \frac{P_{load} - P_{C2}}{P_{Vs}}\end{aligned} \qquad \textit{Eq 6-16}$$

To better understand the relative quantity of the energy circulating between C1 and C2, the energy flows were iteratively calculated for a converter with an average input power (from V_S) of 2kW. The results are shown graphically in Figure 6-9 for DC equivalent points along a $230V_{RMS}$ AC input voltage.

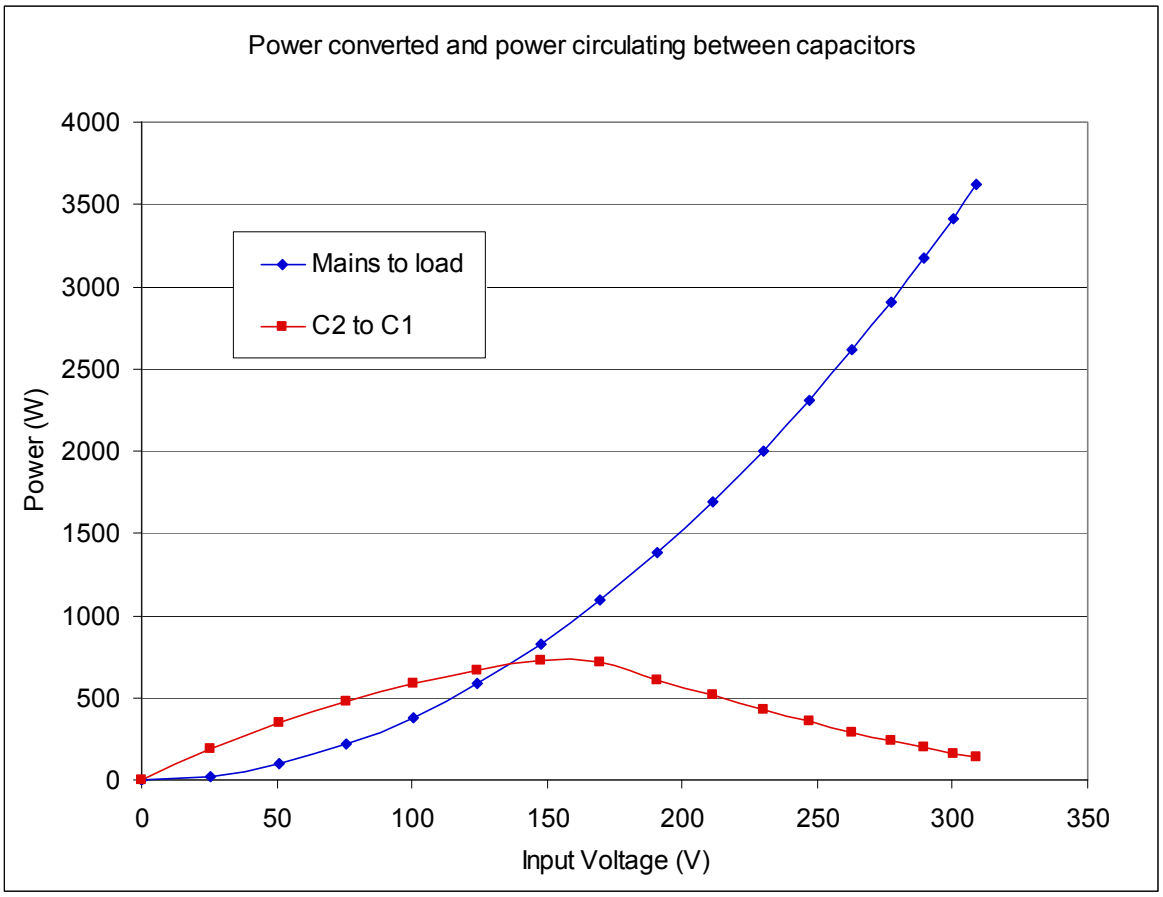


Figure 6-9: Instantaneous useful power converted from the mains to the load compared to the instantaneous power transferring from one capacitor to the other against instantaneous input voltage for an average input power of 2kW

The result of this transfer of power from one capacitor to another is that more current flows through the capacitors and transistors than otherwise would. Ripple current has an effect on the choice of capacitor and transistor current likewise affects the choice of transistor.

6.4 Capacitor Losses in the DC prototype

Figure 6-9 showed that a significant amount of energy circulates between C1 and C2 at 100Hz and peaks when the input voltage is about half the mains peak voltage. This means that significant ripple currents flow through both capacitors in this topology, causing significant losses because of the capacitors' equivalent series resistances (ESRs). These losses were modelled to ensure that the chosen capacitors would not compromise the efficiency of the boost converter.

To achieve a similar cost and physical size as that of a commercial telecommunications power converter, the intention is to construct each of C1 and C2 from two Nippon-

Chemicon ESMQ451VSN181MQ30S 450V 180 µF electrolytic capacitors. These capacitors have a resonant frequency of 60kHz, well below the target switching frequency of 100kHz. To better smooth any switching ripple at the switching frequency (and its harmonics) each electrolytic capacitor was augmented by the addition of a Epcos B32522N6684K 450V 680nF polyester capacitor connected in parallel. Therefore, C1 and C2 each consist of four paralleled capacitors: two 180µF electrolytics and two 680nF polyesters.

To assist with calculating converter performance, the ESR of one of the electrolytic capacitors was measured at 100Hz using a Wayne Kerr 3260B precision magnetics analyser and found to be 374.4mΩ. A polyester capacitor was also measured and found to have an ESR of 34.4mΩ at 100kHz. By numerically modelling the currents that flow through the capacitors, their ESR can be used to calculate the losses that they will cause, as described in sections 6.4.1 through 6.4.4.

Table 6-1 outlines the assumed circuit conditions for the purposes of calculating the capacitor losses.

Capacitance for each of C1, C2	360µF
Inductance of L1	120µH
Switching frequency	100kHz
V_{C1}, V_{C2}	400V
ESR of C1 or C2 at 100Hz	187mΩ
ESR of C1 or C2 at 100kHz	17mΩ
Load	2kW
DC input voltage range	0-325V

Table 6-1: Summary of circuit conditions for modelling capacitor losses

6.4.1 Discontinuous conduction

During discontinuous conduction mode, the current through Q2 and C2 rises from zero while Q2 is on until it reaches some value, I_{pk} at time t_1 when Q2 turns off and the current drops immediately to zero. The current experienced by C2 during the time that Q2 is on, is the same as that experienced by the inductor, L1. In *Eq 6-17*, the RMS of the current through C2 is calculated from t=0 to t=t_1.

$$
\begin{aligned}
I_{C2,R.M.S.(Q2on)} &= \sqrt{\frac{1}{t_1}\int_0^{t_1}\left(I_{pk}\frac{t}{t_1}\right)^2 dt} \\
&= \sqrt{\frac{1}{t_1}\int_0^{t_1} {I_{pk}}^2 \frac{t^2}{{t_1}^2} dt} \\
&= \sqrt{\frac{1}{t_1}\left[{I_{pk}}^2 \frac{t^3}{3{t_1}^2}\right]_0^{t_1}} \\
&= \sqrt{\frac{{I_{pk}}^2}{3}} \\
&= \frac{I_{pk}}{\sqrt{3}}
\end{aligned}
\qquad \textit{Eq 6-17}
$$

The proportion of time during a switching cycle that Q2 is turned on is equal to *D*, the duty cycle so the RMS current from *Eq 6-17* can be used to calculate the average power dissipated in C2 over an entire switching cycle due to high frequency ripple as *Eq 6-18* where R_{C2} is the ESR of the polyester capacitors in C2 at 100kHz.

$$P_{loss(C2)} = \frac{{I_{pk}}^2}{3} \cdot D \cdot R_{C2} \qquad \textit{Eq 6-18}$$

When Q2 turns off, the current that was flowing through C2 with a magnitude of I_{pk} flows through C1 instead. C1's current, therefore, jumps from zero to I_{pk} and then linearly decreases until it reaches zero. The time taken for the current to fall to zero, t_{fall} is calculated using *Eq 6-19*.

$$t_{fall} = \frac{I_{pk} \cdot L}{V_{c1} - V_s} \qquad \textit{Eq 6-19}$$

The RMS current through C1 during this time is, by symmetry, the same as the RMS current through C2 when Q2 was on, expressed in *Eq 6-17*. The total high frequency capacitor ESR losses for both C_1 and C_2 can, therefore, be calculated by multiplying the square of the RMS current, R_C (the ESR of C1 or C2), and the proportion of a switching period that current is flowing through a capacitor. The calculation is shown in *Eq 6-20*.

$$P_{loss} = \left(\frac{I_{pk}}{\sqrt{3}}\right)^2 \cdot R_C \cdot \left(D + \frac{t_{fall}}{T}\right) \qquad \textit{Eq 6-20}$$

6.4.2 Continuous conduction

During continuous conduction mode, a similar approach is taken, however the inductor current when Q2 turns on is some value, I_{base} instead of zero and $t_{fall} = \frac{1-D}{f}$.

The combined losses in capacitors C1 and C2 at the switching frequency are calculated as

$$P_{loss} = \left(\frac{I_{pk-pk}}{\sqrt{3}} + I_{base}\right)^2 \cdot R_C . \qquad \textit{Eq 6-21}$$

$I_{pk\text{-}pk}$ is calculated in the same way as I_{pk} was for DCM, however, the minimum current is non-zero which results in a peak-to-peak value rather than a peak or maximum. Because the current ripple occurs at the switching frequency, the ESR of the polyester capacitors at 100kHz is used for R_C (17.2mΩ).

6.4.3 Low frequency capacitor losses

In addition to the high frequency ripple currents that flow in C1 and C2, over longer periods of time spanning many switching cycles, the power flowing from the mains varies whilst the power drawn by the load remains constant. The difference is largely made up for by the electrolytic capacitor components of C1 and C2.

During positive half-cycles, C1 absorbs significant amounts of energy near the peak of the mains and supplies significant amounts near the zero crossings. During negative half cycles, the same is true for C2. By calculating the difference in power flowing into the circuit from the mains and out to the load, the power absorbed or supplied by the electrolytic capacitors can be calculated. This power transfer value can then be used to calculate the approximate current flowing through the electrolytic capacitors by assuming negligible voltage ripple occurs. The losses in the electrolytics are calculated based on the current flowing through them and the ESR measured at 100Hz.

6.4.4 Total capacitor losses

The duty cycle, voltages and currents in the circuit were iteratively calculated at points spaced 0.25ms apart over a mains quarter-cycle. At each point the power dissipated because of high frequency ripple in the polyester capacitors and thus, low frequency ripple in the electrolytic capacitors was calculated. The results of these calculations are shown in Figure 6-10. The losses due to low frequency ripple are larger at low voltages where C1 supplies most of the load and at high voltages where C1 is recharged near the peak of the mains. The minimum occurs where the average energy stored by C1 over a switching period is zero, because the sum of the input power and power provided by C2 equals the sum of the load power and losses.

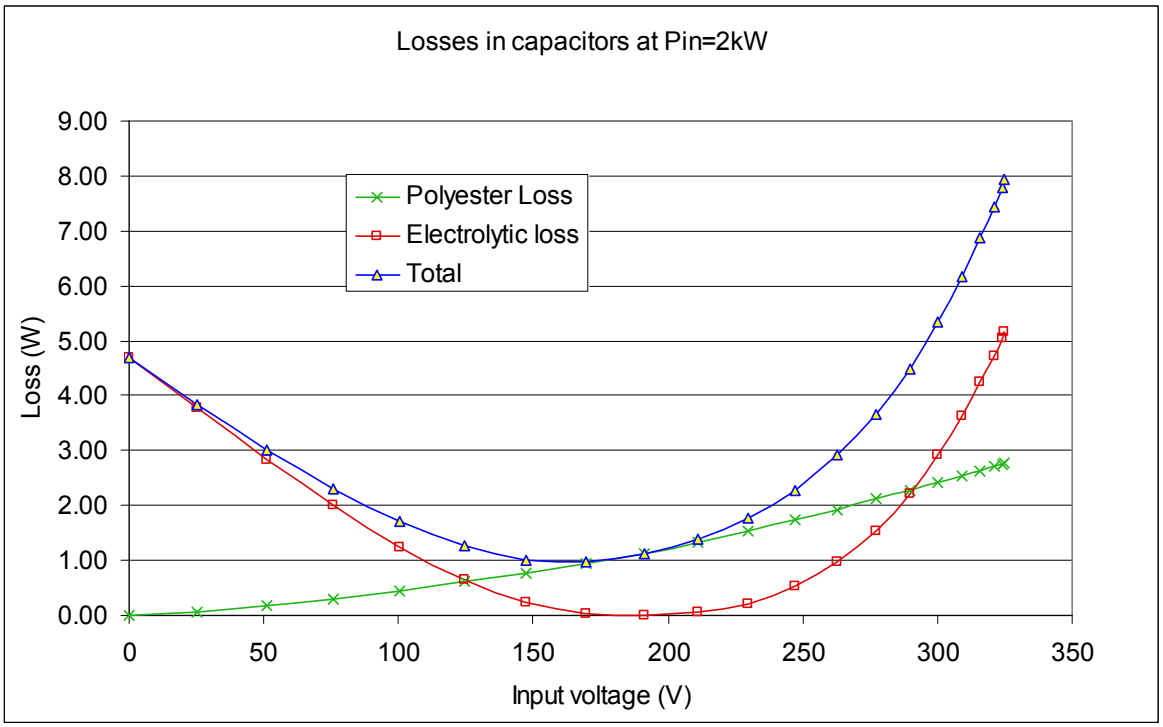


Figure 6-10: Instantaneous combined losses in C1 and C2 at 2kW average converter power

Integrating the capacitor losses in Figure 6-10 over a mains quarter-cycle using points evenly spaced in time, allows the average power dissipated by the capacitors to be calculated. The results are summarized in Table 6-2.

Capacitor	P_{loss} (W)	P_{loss}(%)
Electrolytic	2.23	0.11%
Polyester	1.49	0.07%
Total	**3.71**	**0.19%**

Table 6-2: Average power dissipated by the different types of capacitor comprising C1 and C2

6.5 Transistor Losses

6.5.1 Transistor conduction losses

It is assumed that sufficient dead time is implemented by the control circuitry that shoot through does not occur and that the mains current only flows through one transistor (or its anti-parallel or body diode) at any time. The currents flowing through C1 and C2 are also the currents that flow through Q1 and Q2, so the models for these currents in sections 6.4.1 for discontinuous conduction mode and in 6.4.2 for continuous conduction mode can be used to calculate the conduction losses in Q1 and Q2.

In the case of Q1, synchronous rectification is achieved if Q1 is turned on by the control circuitry when current is flowing through it. For larger currents, a SiC Schottky diode connected in anti-parallel with Q1 could offer a lower voltage drop than Q1's channel. To investigate this, the losses that would occur (such a diode be used and Q1 kept off) were calculated for an assumed constant diode forward voltage drop of 1.6V.

The losses for Q1 and Q2 and Q1's anti-parallel diode, D1 are shown in Figure 6-11 for a 2kW converter based on the SDA10S120 SiC Schottky diode from SemiSouth. Best and worst case scenarios are also shown on the graph. The best case scenario assumes an optimistic 150mΩ $R_{DS(on)}$ and the worst case assumes a pessimistic 250mΩ $R_{DS(on)}$. For the overall circuit performance model, synchronous rectification is used wherever it provides an advantage over the losses that would occur with D1.

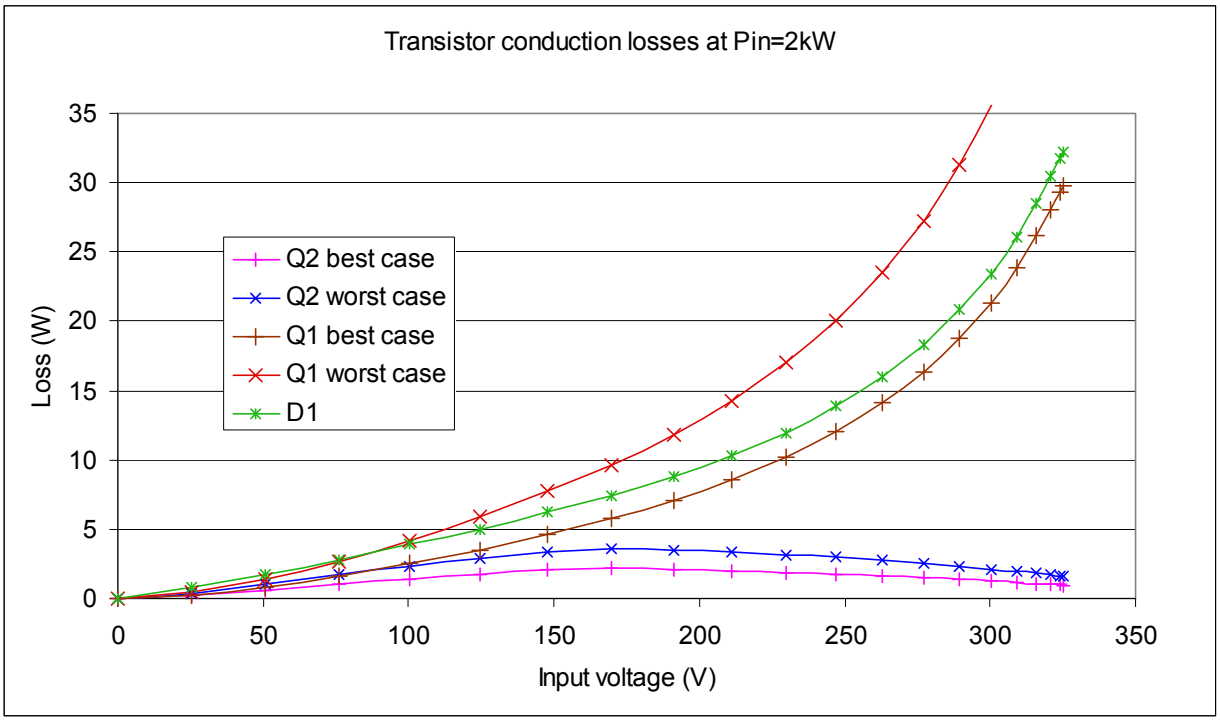


Figure 6-11: Instantaneous conduction losses at 2kW for each transistor and the anti-parallel diode, D1 at various points on the mains waveform.

6.5.2 Transistor Drive Losses

To keep one of the SJEP120R125 JFETs turned on, a sustained gate current is required. To conduct drain currents in excess of 18A, it is estimated from Appendix C that approximately 100mA of gate current will be required at a gate-source voltage of 3V. Assuming that one transistor is on at any time, the approximate power required to continuously bias the transistors is 0.3W. In addition to the continuous drive, short pulses of high current need to flow in and out of the gate to achieve fast transitions. The gate charge of 25nC suggests that the energy which must be transferred into a SiC JFET at turn-on is

$$E = \frac{1}{2}QV = \frac{1}{2}\cdot 25\times 10^{-9}\cdot 3 \ = 112.5nJ\,. \qquad Eq\ 6\text{-}22$$

From *Eq 6-22* the power required to charge the gate of a transistor at turn-on at a switching frequency of 100kHz is 11.25mW. Therefore, the overall transistor drive loss for both transistors is 0.32W.

6.6 Inductor losses

The inductor chosen is a 120µH component that was custom designed for use by Eaton Corp in a 2kW power factor correction application. Because the switching frequency of the SiC PFC is to be similar to that of Eaton's product and the average current identical, it was made a design goal to utilise the exact same 120µH component.

The inductor has a core size, type and gap chosen to maximize energy storage without allowing saturation to occur. To minimize skin effect, the inductor's windings are fabricated from Litz wire. The inductor was measured using a Wayne Kerr 3260B precision magnetics analyser and the sample used in Chapter 8 and shown in Figure 6-12 was found to have an inductance of 122µH and an equivalent series resistance of 80mΩ at 100kHz.

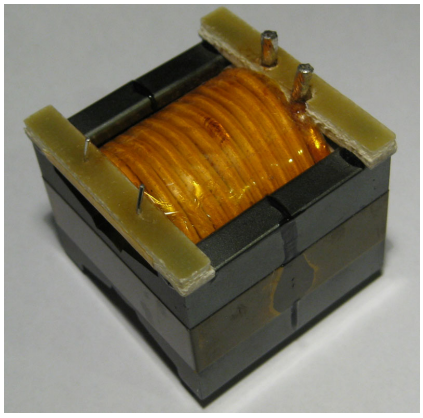


Figure 6-12: 120µH inductor for PFC

The RMS current through the inductor during continuous conduction mode is the sum of the current through Q1 and Q2, described by *Eq 6-23* where I_{base} is the minimum current magnitude (which occurs when Q2 turns on) and $I_{pk\text{-}pk}$ is the peak to peak switching frequency ripple current.

$$I_{L(R.M.S.,CCM)} = \sqrt{\frac{t_2}{T}\left[I_{base}{}^2 + \frac{I_{base} I_{pk-pk}}{2} + \frac{I_{pk-pk}{}^2}{3} \right]} \qquad \textit{Eq 6-23}$$

During discontinuous conduction mode, the current through the inductor is also the sum of the currents through Q1 and Q2 as expressed by *Eq 6-24* where t_2 is total time during which either Q1 or Q2 is conducting.

$$I_{L(R.M.S,DCM)} = I_{pk} \cdot \sqrt{\frac{t_2}{3T}} \qquad \textit{Eq 6-24}$$

The resistive losses in the inductor's windings were calculated using Ohm's law from *Eq 6-23* and *Eq 6-24* for a 2kW converter and are shown graphically in Figure 6-13 against input voltage.

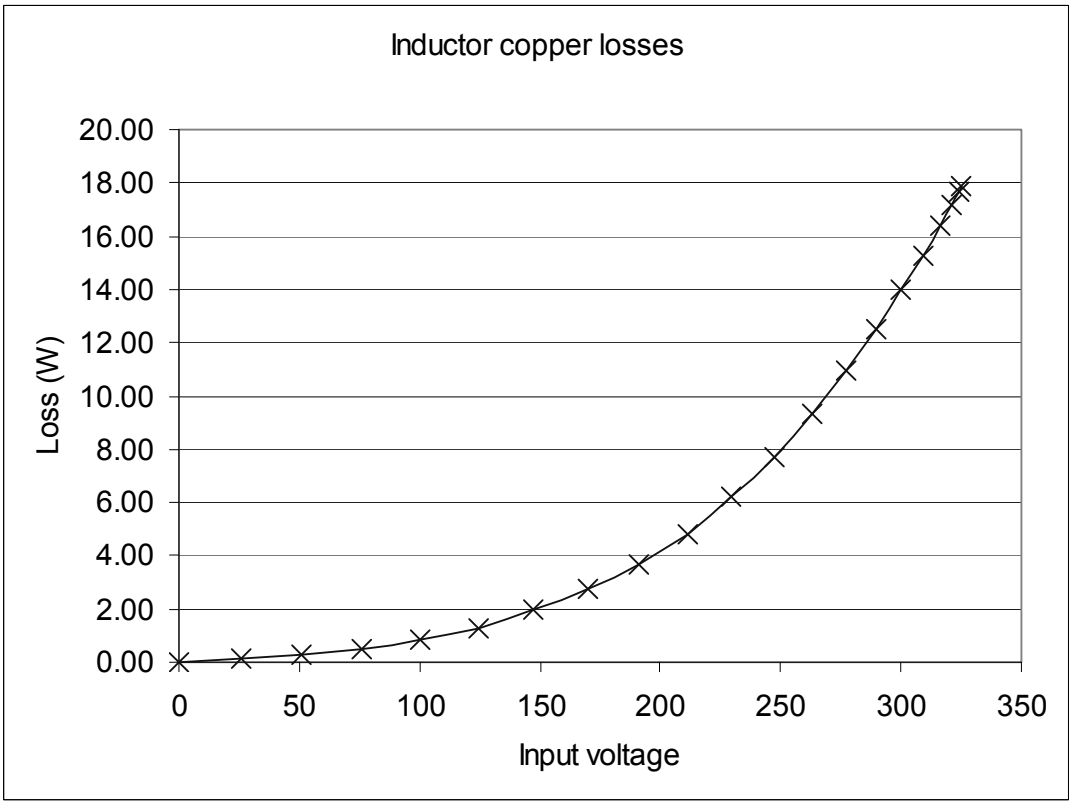


Figure 6-13: Resistive losses in the inductor against instantaneous input voltage for a 2kW converter

The points in Figure 6-13 were spaced evenly in time every 0.25ms along a mains quarter-cycle. This allows the inductor's average resistive loss to be calculated as the simple average of the data points. The result is 7.68W or 0.38% of the 2kW input power.

6.7 Combined conduction losses

The capacitor, inductor and transistor conduction losses for the PFC circuit in Figure 6-1 were each calculated for a 2kW converter and are summarized and totalled in Table 6-3.

Conduction Loss	Absolute (W)	Proportion (%)
Electrolytic capacitors	2.23	0.11%
Polyester capacitors	1.49	0.07%
Transistors (worst case)	16.50	0.82%
Transistors (best case)	13.95	0.70%
Inductor	7.68	0.38%
Total (worst case)	**27.90**	**1.40%**
Total (best case)	**25.35**	**1.27%**

Table 6-3: Summary of average conduction losses for a 230V converter at 2kW output power

6.8 Switching Losses

6.8.1 Datasheet approximation

Methods for modelling the switching losses of a silicon MOSFET have been published, [124] but a similarly detailed technique is not available for normally-off SiC JFETs. Some information about SiC JFET switching losses is provided in the manufacturer's datasheet under certain conditions [Appendix C]. The information includes turn-off energy (E_{OFF}), turn-on energy (E_{ON}) and their sum (E_{TS}). This information has been reproduced in Figure 6-14 alongside a linear approximation of it. The approximation takes an average of the 25°C and 150°C and is used for estimating the turn-on losses during continuous conduction mode and the turn-off losses in both continuous and discontinuous conduction modes.

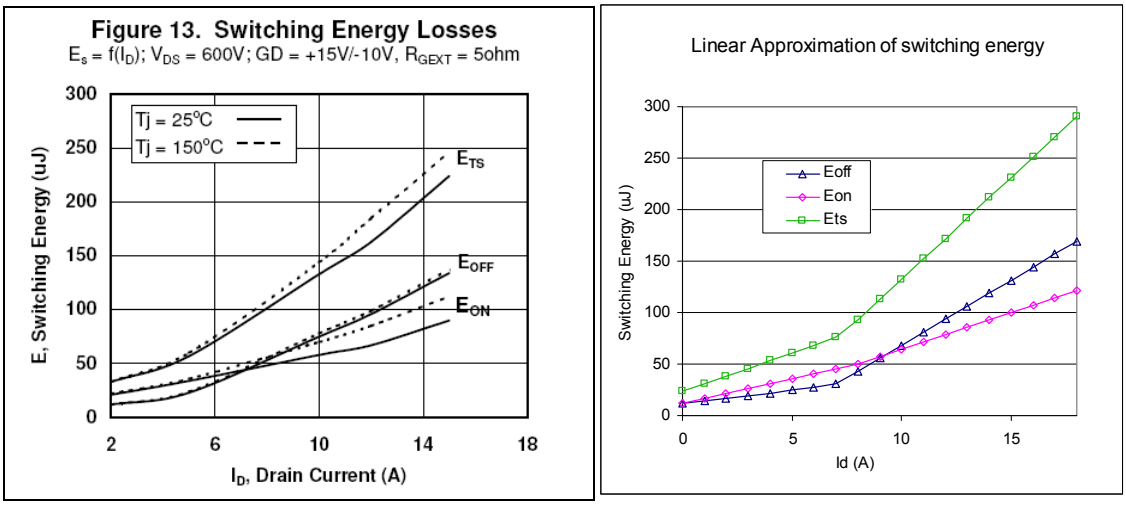


Figure 6-14: Switching energy losses for the SJEP120R125 reproduced from [Appendix C] (left) and the proposed linear approximation for modelling (right)

The linear piecewise approximation in Figure 6-14 for turn-off energy is given by *Eq 6-25*.

$$E_{off} = \begin{cases} (7 + 2.5 \cdot I_D) \times 10^{-6} & I_D < 6.4 \\ (23 + 12.6 \cdot (I_D - 6.4)) \times 10^{-6} & I_D > 6.4 \end{cases} \qquad \textit{Eq 6-25}$$

The linear piecewise approximation for turn on energy is given in *Eq 6-26*.

$$E_{on} = \begin{cases} (12 + 4.75 \cdot I_D) \times 10^{-6} & I_D < 8 \\ (50 + 7.1 \cdot (I_D - 8)) \times 10^{-6} & I_D > 8 \end{cases} \qquad \textit{Eq 6-26}$$

The switching losses in Figure 6-14 are for a drain-source voltage of 600 volts. The voltage experienced in the PFC circuit is the combined voltage that appears across C1 and C2, approximately 800V. To incorporate this difference into the PFC circuit model, *Eq 6-25* & *Eq 6-26* linearly scaled by a factor of $\frac{800}{600}$. The assumption of a linear relationship between blocking voltage and turn-on loss is based on MOSFET implemented based buck converters in [125] where the turn-on loss was proportional to the product of blocking voltage, conduction current and current rise time. It was found in [125] that rise time was largely attributed to gate drive characteristics, which in the prototype circuit presented in Chapter 7 have superior peak current capability than the +15/-10V supply and 5Ω impedance network used when generating the curves in Figure 6-14.

The turn-on, turn-off and total switching losses are shown in Figure 6-15 based on the data from Figure 6-14.

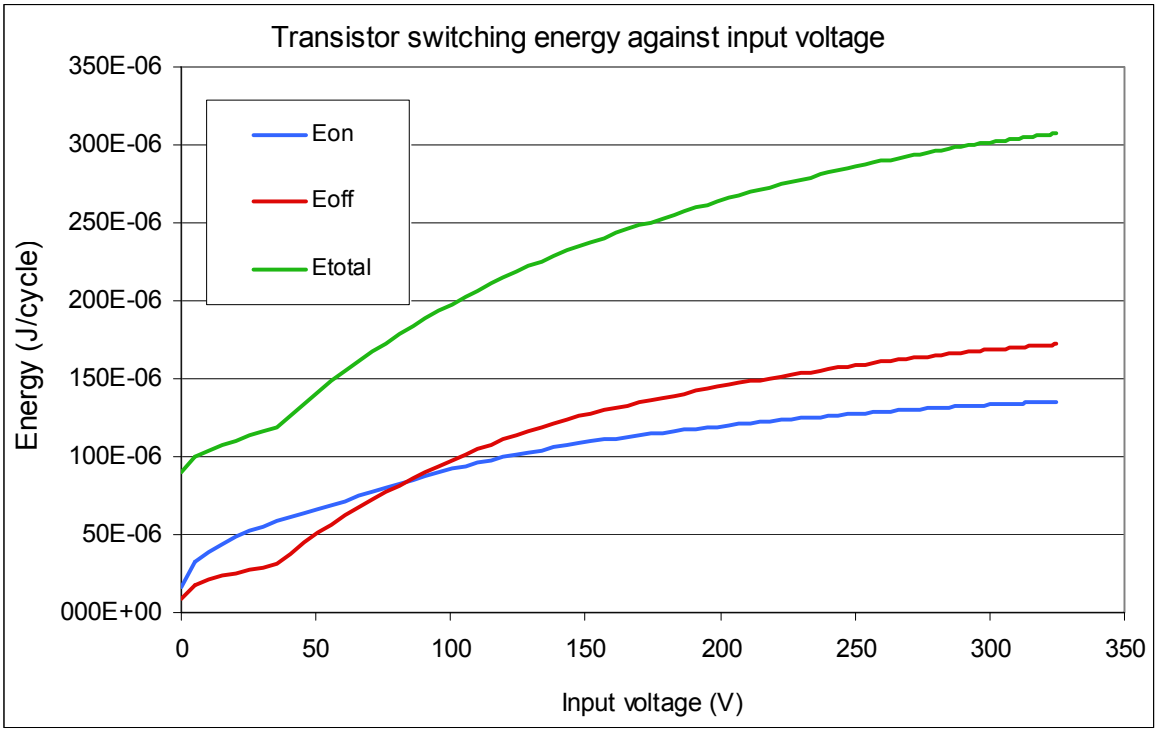


Figure 6-15: Transistor switching energy per cycle at 2kW

6.8.2 Turn-on during DCM

During discontinuous conduction mode, after Q2 turns off, the current through the inductor decreases linearly to zero before Q2's next turn-on. Upon reaching zero current, until Q2 turns on, resonance occurs between the inductor and various parasitic capacitances, particularly the drain-source capacitances of the JFETs. The resonance causes the voltage across Q2's drain-source to oscillate, resulting in a range of possible drain-source voltages at the moment of Q2 being turned on. If Q2 is able to be turned on near one of the local minima in the oscillating drain voltage, the turn-on is almost entirely lossless. The best case model therefore assumes a turn-on loss of zero in discontinuous conduction mode, while the worst case model assumes that a hard turn-on occurs at the peak of the oscillations and the turn-on loss is calculated by linearly scaling by the worst case voltage appearing across Q2.

6.8.3 Diode losses

During continuous conduction mode, Q2 experiences lossy hard turn-on and turn-off transitions. Switching losses in Q1 are assumed to be zero because as a synchronous rectifier, Q1 turns on with only D1's forward voltage drop across Q1 and turns off as the current through Q1 reaches zero due to Q2 turning on. The forward voltage drop of D1 is

sufficiently small for any turn-on losses of Q1 to be negligible and turn-off transitions occur with close to zero current through Q1 if the timing of Q1's turn-off signal is sufficiently precise. Losses due to reverse recovery of the anti-parallel SiC Schottky diode (which conducts briefly during dead time) are assumed to be negligible.

The diodes used are SDA10S120 SiC diodes manufactured by SemiSouth. The manufacturer claims that these devices have "zero reverse recovery current" and "zero forward recovery voltage" [126] suggesting that losses due to forward and reverse recovery are negligible. [126] also graphs the stored energy against reverse voltage. This graph, reproduced in Figure 6-16 shows that at 800 volts, the SDA10S120 stores approximately 12.7μJ. If this energy is the only switching loss associated with the rectification process, the loss at 100kHz is 1.27 watts.

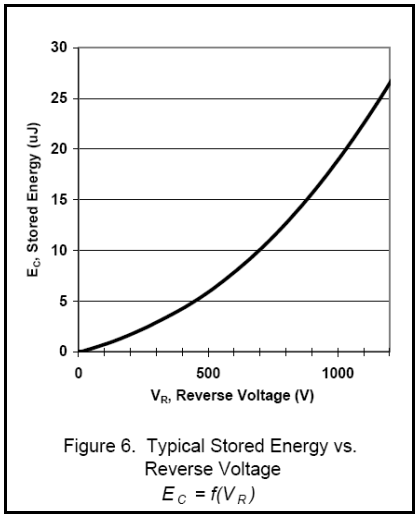


Figure 6-16: Stored energy in the SDA10S120 SiC Schottky diode, reproduced from [126]. Approximately 12.7uJ is stored at 800V

6.9 Results of circuit model

All losses discussed in this chapter were calculated at 21 operating points spaced 0.25ms apart over a mains quarter-cycle. Because of the uncertainty over the exact equilibrium junction temperature, both the best and worst case temperature scenarios were calculated separately based on 25°C and 150°C respectively. The assumption that the junction temperature lies between 25°C and 150°C is supported by the thermal design of a prototype circuit in Section 7.1. It was also assumed for the best case scenario, that Q2

achieves lossless turn-on during discontinuous conduction mode while the worst case assumes that Q2's turn-on is entirely hard-switched.

Table 6-4 provides a summary of the sinusoidally weighted loss for each individual component for the best and worst case scenarios. The total losses can be used to calculate the expected overall efficiency range of the PFC circuit as 97.0 - 97.4%.

Conduction Losses	**W (best case model)**	**W (worst case model)**
Electrolytic capacitors	2.23	2.23
Polyester capacitors	1.49	1.49
Transistors	13.95	16.50
Inductor	7.68	7.68
Switching Losses		
Turn-off	16.17	16.17
Turn-on	9.62	13.60
Diode charge	1.27	1.27
JFET drive losses	0.32	0.32
Total	52.73	59.26
Efficiency	97.4%	97.0%

Table 6-4: Summary of all calculated losses for the revised PFC model at 2kW

The efficiency curves predicted by the best and worst case models as well as their average (half way between) are shown in Figure 6-17 against input voltage with data points spread 0.25ms apart over a mains quarter-cycle. The gap between the best and worst case models substantially narrows above 160V as the circuit enters continuous conduction mode and zero voltage turn-on no longer occurs with the best case model.

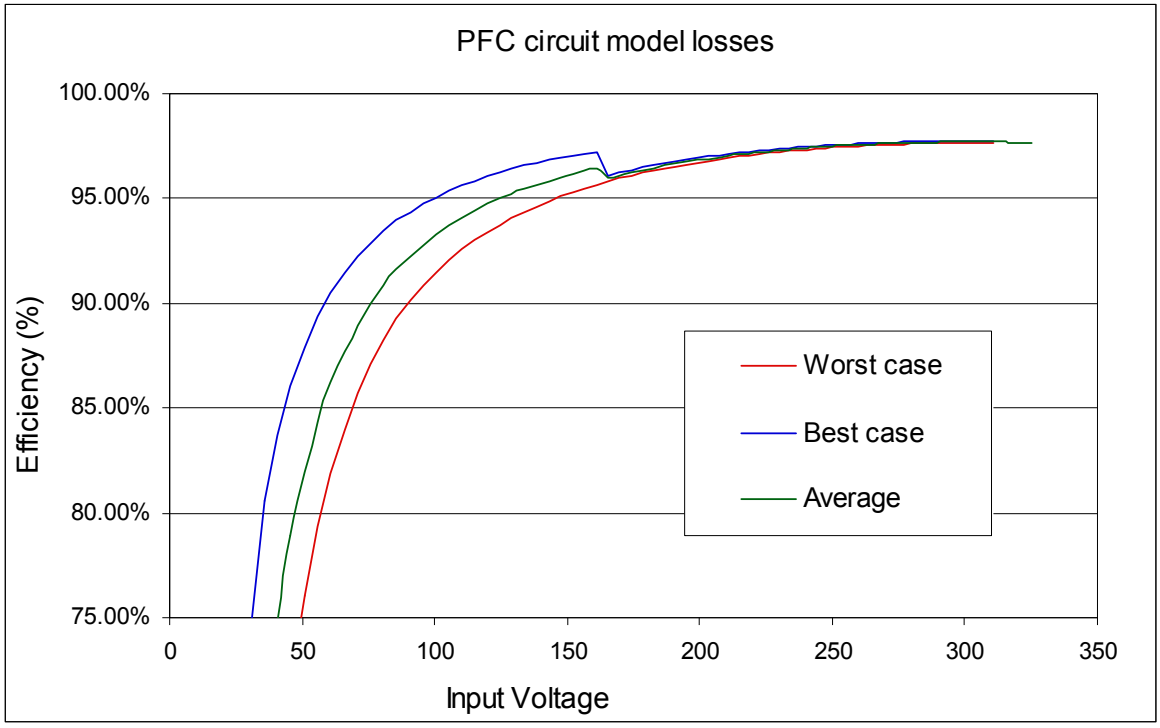


Figure 6-17: The PFC circuit's instantaneous conversion efficiency predicted by the best and worst case models

6.10 Conclusions

A topology expected to benefit from the use of SiC JFETs was selected. The operation of this topology was explained in detail with the aid of its DC equivalent circuit. The circuit's voltages and currents were calculated for points along the AC input sinusoid. At every point, losses were calculated for each component in the circuit. The points were weighted to allow an average loss to be calculated for each component as well as the overall circuit.

Due to the dependency between $R_{DS(on)}$ and temperature, coupled with the limited available data for the new SiC JFETs, some uncertainty existed over the final equilibrium temperature (and therefore $R_{DS(on)}$ likely to be experienced in this application. To mitigate the uncertainty, the performance predictions were duplicated under two different thermal scenarios. One scenario took a very optimistic approach, assuming a very low junction temperature while the other scenario assumed a very high junction temperature. These scenarios resulted two different sets of performance predictions referred to in this thesis as the best and worst case predictions. The real world performance is expected to lie between these two sets of predictions as will be verified in Chapter 8. The predicted overall efficiency for the PFC was 97.0% for the worst case and 97.4% for the best case scenario.

Chapter 7 PFC DC equivalent prototype design

To test the actual performance of the power factor correction circuit proposed in Chapter 6, a prototype of its DC equivalent circuit was designed to be of similar structure to that used in Figure 6-2 for mathematical modelling purposes. To meet the desired performance targets, a number of design decisions were made, often compromising between different losses to achieve good overall performance.

7.1 Thermal design

The transistors used are SemiSouth SJEP120R125 'normally-off' SiC JFETs, packaged in TO-247 cases. Whilst multiple devices could be connected in parallel to achieve lower conduction losses and thermal impedance, this would cause too great an increase in switching losses, so one device was used for each switch. The prototype PFC circuit was sized as a 2kW converter and optimised for electrical efficiency at an input of 1600W. When losses are accounted for, this is just under 80% load, a figure considered to be an accurate reflection of common usage from the high utilisation of conversion capacity with some head room.

In Section 6.5, two mathematical models were presented for the conduction losses in the transistors. Lumped together, the two JFETs dissipated 16.50W in the worst case model and 13.95W in the best case. Switching losses were then modelled in Section 6.8, with best and worst case values of 26.11W and 30.09W respectively.

The resistance vs temperature characteristic of the SJEP120R125 JFET in Figure 7 of Appendix C is relatively steep, suggesting that a large heat sink will significantly improve overall efficiency by reducing the conduction losses substantially. Physically large heat sinks are not desirable in the target application, but existing designs utilize forced-air cooling, allowing very low thermal impedances to be achieved without excessively large heat sinks. Therefore, it is reasonable to assume that an equivalent thermal impedance of 1.2°/W can be achieved.

If both transistors are attached to the same 1.2°/W heat sink, it is assumed that in steady state, the thermal circuit is the equivalent of the transistors' combined losses being conducted through their parallel junction to case and case to heat sink impedances (T_{JC} and

T_{CH} respectively) and the single heat sink to ambient impedance T_{HA}. The overall thermal impedance is represented by *Eq 7-27*

$$Z_T = \frac{T_{JC}}{2} + \frac{T_{CH}}{2} + T_{HA} \qquad \textit{Eq 7-27}$$

The case to heat sink thermal impedance, T_{CH} for a TO-247 package with a silicone insulating pad is assumed to be approximately 0.3°/W and [Appendix C] states that T_{JC} for the SJEP120R125 is 1.1°/W. From *Eq 7-27*
, the total thermal impedance can be calculated as shown in *Eq 7-28*. In the worst case scenario, the total transistor dissipation (switching, conduction and drive losses) is 46.59W, resulting in a junction temperature rise of 88.5° above ambient, or 113.5°C at an ambient temperature of 25°C. This is less than the 150°C temperature that was assumed when calculating a $R_{DS(on)}$ of 250mΩ in 6.5.1 for the worst case model, suggesting that the actual junction temperature will be less. It is also significantly less than the 175°C absolute maximum rating of the SJEP120R125's junction. The same calculations for the best case model result in a junction temperature of 100°C.

$$Z_T = \frac{1.1}{2} + \frac{0.3}{2} + 1.2 = 1.9°/\text{W} \qquad \textit{Eq 7-28}$$

7.2 Output Stage

The output stage, shown in Figure 7-1 is relatively simple, based on a half bridge formed by Q1 and Q2, the two SiC JFETs. The circuit operates from DC voltage source, V_{mains} which simulates a single point in the mains sinusoid. Q2 provides switching while D1 rectifies with Q1 also allowing synchronous rectification to be used. D2 does not conduct but is present in the AC PFC circuit and included in the DC equivalent to ensure that its parasitic capacitance is modelled.

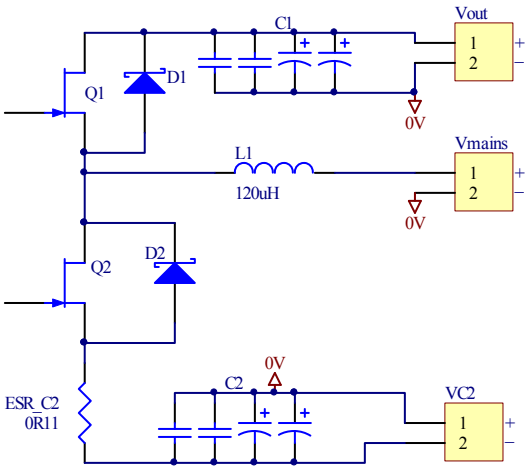


Figure 7-1: Output stage of the PFC circuit's DC equivalent

To measure currents of interest, two options exist, namely measuring the voltage drop across a shunt or the use of a loop of wire with a Hall effect sensor. The high currents in the circuit dictate that the resistance of a shunt must necessarily be very low to avoid significant losses. Practical values of less than 100mΩ result in very small voltage drops at low power, such that the signal to noise ratio of a differential measurement is likely to be unacceptably low. As a result, it was decided that small loops of wire would be used with Hall effect sensors, despite the extra inductance that these loops introduce. To mitigate the inductance, the loops are kept only as large as required to fit into the jaws of a typical oscilloscope current measuring Hall effect probe. Careful PCB layout further minimizes the inductance by taking advantage of the wire loops to cover some of the distance that would already need to be traversed between physically large components' terminals. The minimum width requirement of the probe jaws also allows any perpendicular PCB traces to be wider. The resulting implementation has sufficiently low inductance to be considered fit for purpose.

7.3 C2 equivalent

In the DC equivalent circuit, C2 is represented by a DC voltage source. The same electrolytic and polyester capacitors are used for C1 and C2, but the use of a DC source to represent the available stored energy in C2 does not correctly account for the losses associated with the internal resistance of C2. To include these losses in the DC equivalent prototype circuit, a resistor, represented by R_C2 in Figure 7-1 was included. At low frequencies, the ESR of C1 or C2 is much larger than at high frequencies.

In section 6.4, the ESR of a Nippon-Chemicon ESMQ451VSN181MQ30S capacitor was measured using a Wayne Kerr 3260B precision magnetics analyser as being 374mΩ at 100Hz. The ESR of a Epcos B32522N6684K polyester capacitor was measured as being 34.4mΩ at 100kHz on the same analyser. Two of each capacitor type were connected in parallel, resulting in an ESR of less than 187mΩ at 100Hz and less than 17.2mΩ at 100kHz. Because the current through C2 contains a mixture of high and low frequency components, a resistance of 110mΩ was chosen to approximate the losses that occur in these ESRs. For power handling, the resistor was constructed from three paralleled 330mΩ 1W resistors in 2512 packages.

7.4 Driver Stage

7.4.1 Rapid switching

To minimize switching losses, it is important to ensure that the JFET turn-on and turn-off transitions are as brief as possible. While around 100mA is sufficient to maintain the SJEP120R125 in a sufficiently low resistance conducting state, a larger gate current will decrease the time required to transition from blocking to conducting. It was recommended in [108] that a very large current be driven briefly through the gate of a JFET to turn it on rapidly before maintaining the gate current at lower levels. It is important that the high current pulse is brief because once the JFET is conducting, excessive gate current will result in unnecessary losses and could damage the JFET's gate structure.

To achieve the high current pulse requirement in addition to the lower continuous current drive, a dual driver arrangement is used as suggested in [108]. It is intended that a saleable product would incorporate the novel bootstrap arrangement proposed in Chapter 5 potentially with a DC-coupled two-stage output. However, for laboratory simplicity, a floating power source shall be used in this prototype. The drive circuit is shown in Figure 7-2. Driver A in U1 is driven with a conventional square PWM waveform. R2 and R3 limit the continuous gate current to approximately 70mA. D2 provides a lower impedance return path for the gate current to achieve rapid turn-off, with R1 damping the inevitable ringing. To achieve a fast turn-on transition, a brief pulse is driven through driver B of U1. R4 limits the pulse current to a safe value and dampens ringing, while D3 prevents driver B from pulling the gate voltage low at the conclusion of the short pulse.

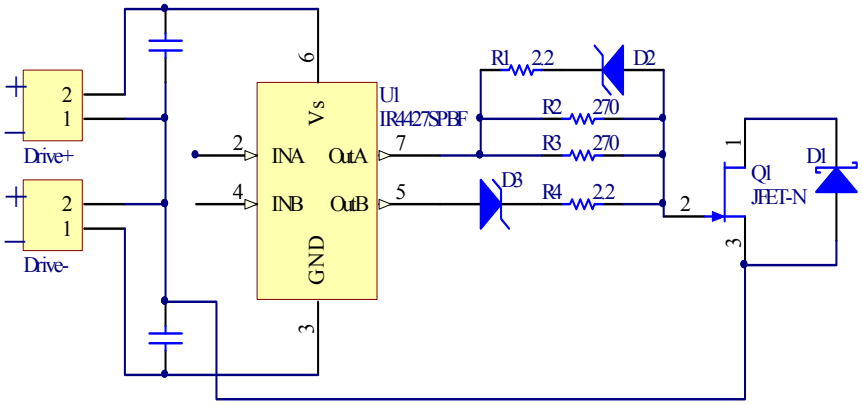


Figure 7-2: Single JFET gate drive circuit for the PFC prototype

The author and [108] observed undesired turn-on behaviour when two SJEP120R125 JFETs were used in other circuits with bridge configurations. A negative gate voltage at turn-off was described as a solution in Chapter 4. A similar approach was taken to protect against cross-conduction in the PFC prototype circuit by powering each driver IC from a split supply. The source of each JFET was connected to the midpoint of each split supply and the supplies were well decoupled to keep their AC impedance as low as possible.

To keep the propagation and transition times equal, the same floating split supply arrangement was used for both the upper and lower JFETs in the output bridge. The complete output bridge and gate drive including additional decoupling capacitors and support circuitry is shown in Appendix B, Schematic 4.

7.4.2 High Voltage Level-Shifting

The upper JFET and its drive circuit float to as much as 325V at the peak of a mains half-cycle, while lower JFET's source is at a potential of −400V DC. Although it would be possible to only use level shifting circuitry on the upper JFET's PWM signal by referencing the -400V node to ground, the mismatch in propagation delays between the level shifted and non-level shifted PWM signals would have been unacceptably high. It was therefore decided that this option not be implemented, and that level shifting circuitry be used for both the upper and lower JFETs' PWM signals.

The level-shifting of each PWM signal is achieved by an ADUM2400 magnetic coupler, manufactured by Analog Devices. The ADUM2400 contains four air-cored transformers for electrical isolation as well as special circuitry on both sides of each transformer. The

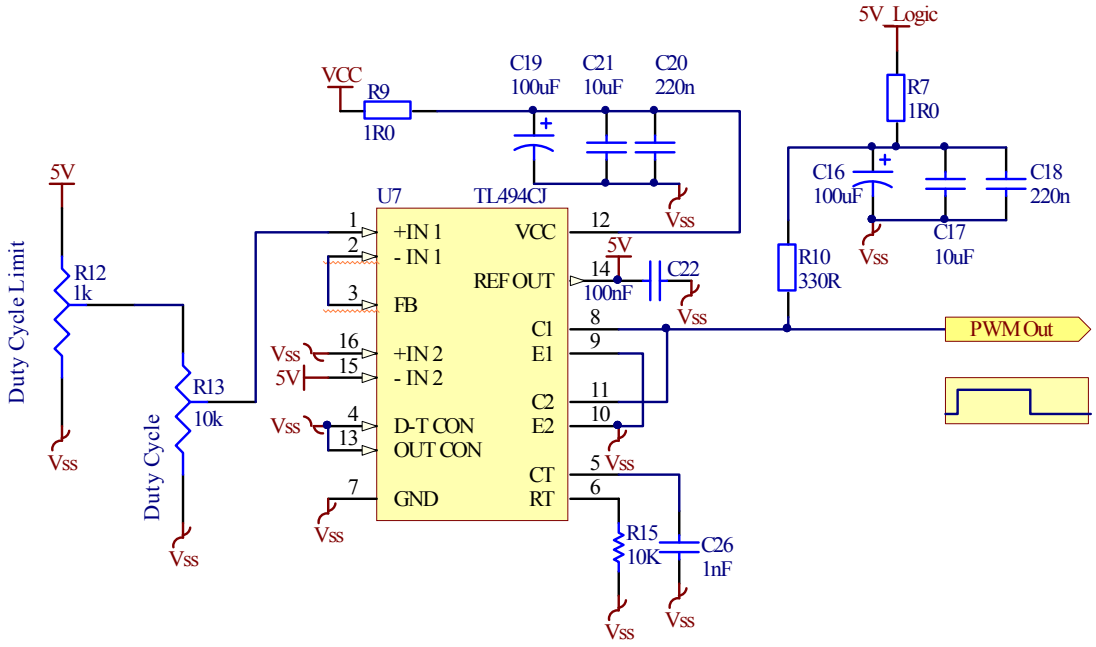
circuitry provides buffering with Schmitt trigger-like characteristics as well as a special signalling system that allows DC signals to be transmitted, unlike passive pulse transformers.

The driver circuits for the two JFETs each require a separate ADUM2400 because of the differing potentials to which the PWM signals need to be shifted. Each JFET requires two channels from its ADUM2400: one for the PWM signal and one for the short turn-on pulses. The two channel ADUM2200 could also have been used, but these devices were not available.

A floating five volt power supply is derived from each floating gate drive power supply by a linear regulator and connected to the high voltage side of each ADUM2400. The ADUM2400s' low voltage sides are powered by the same 5V supply that powers the pulse-shaping logic circuits.

7.5 Pulse width modulation and pulse-shaping

To drive the JFETs in the bridge at the correct times, a square wave signal is required. A TL494 is used to generate this signal with a variable duty cycle to control the boost ratio. Figure 7-3 shows the PWM circuit in its entirety. R12 allows the maximum duty cycle to be limited, which in turn limits the maximum boost ratio . R13 allows the duty cycle to be varied from zero to the maximum duty cycle. R15 and C26 set the frequency of the PWM signal at approximately 100kHz. The TL494 operates from a 12V DC supply rail but its output is made compatible with TTL devices by only pulling it up to a well decoupled 5V rail via R10.



Variable duty cycle PWM @ 100kHz

Figure 7-3: Pulse width modulation signal generator

To create precisely controlled turn-on pulses as well as dead time, the PWM signal is fed through a pulse-shaping circuit shown in Figure 7-4. The signal is initially inverted by U5A, a Schmitt NAND gate before being fed into U5B and U5C. U5B creates a non-inverted version of the PWM signal, while TR2, R11 and C24 form a delay, causing U5C to output non-inverted version of the PWM signal with a slight delay compared to U5B's output.

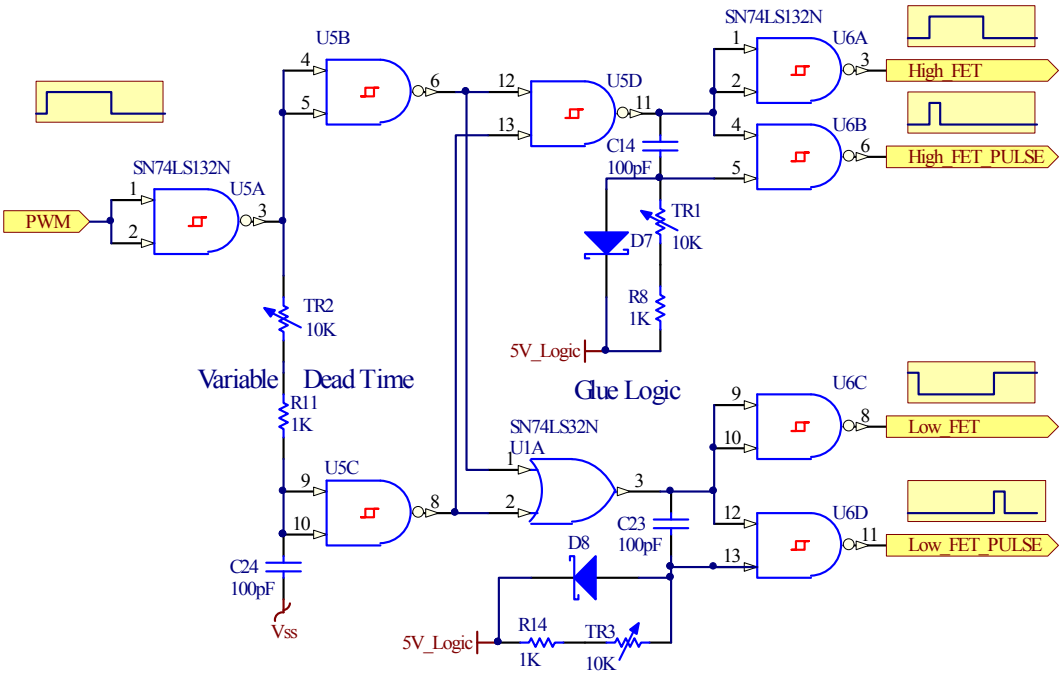


Figure 7-4: Pulse-shaping logic circuitry

The two slightly out of phase PWM signals are fed into the inputs of U5D and U1A. U5D, a Schmitt NAND gate, compares the two inverted PWM signals and goes low only when both inputs are high. U1A, on the other hand, goes low whenever both signals are low. The result is that U5D produces an inverted PWM signal with slightly higher duty cycle than the original PWM signal, while U1A produces a non-inverted version of the PWM signal which also has a slightly higher duty cycle. The upper JFET's PWM signal undergoes another inversion in U6A to produce a signal of the correct polarity and U6C provides the final inversion for the lower JFET's PWM signal.

With the final inversions, the duty cycles of both upper and lower JFETs are slightly lower than were dictated by the PWM signal. This creates dead time to protect against shoot-through in the JFET bridge.

The network formed by C14, TR1, R8 and D7 operates as a falling edge detector, generating short pulses whenever the upper JFET's PWM signal, High_FET, transitions high. Similarly, C23, R14, TR3 and D8 detect when the lower JFET's PWM signal, Low_FET, transitions high and creates a short pulse. These logic signals are able to control the JFET drive circuits in Figure 7-2.

The implementation of the pulse-shaping circuit has been designed to minimize the difference in propagation time between the four outputs at the expense of overall propagation time and total number of logic gates. The circuit allows independent adjustment of dead time, upper JFET turn-on pulse length and lower JFET turn-on pulse length via TR2, TR1 and TR3 respectively. It was suggested in [108] that a pulse length of approximately 100ns is required, so the pulse and dead time circuits were designed to be adjustable over a range of a few tens of nanoseconds to several hundred nanoseconds.

The complete PWM and pulse-shaping circuits are shown together with decoupling capacitors and support circuitry in Appendix B, Schematic 5.

7.6 High Speed design considerations

In addition to matching the propagation delays of the logic signals through the pulse-shaping and level-shifting circuits, many other aspects are important to ensuring that the PFC circuit performs well at high switching frequencies. As a result of the high slew rate of the voltage between the input and output of the ADUM2400, extremely good decoupling is implemented on both sides to minimize the injection of interference into the low voltage logic signals. The data traces are resistively terminated at the non-driving end to reduce transmission line reflections.

Good design practices were followed throughout the prototype with regard to layout and decoupling. A variety of high quality capacitors were used to attenuate noise over a broad frequency range and to supply short term transient loads where required.

7.7 PCB Layout

A multilayer composite view of the PFC prototype circuit's PCB is shown in Figure 7-5 with the ground planes hidden for clarity. The board has only two copper layers to minimize cost and allow in-house fabrication. It carries through-hole components on one side and surface mount components on both sides. Power and data traces were kept perpendicular wherever possible.

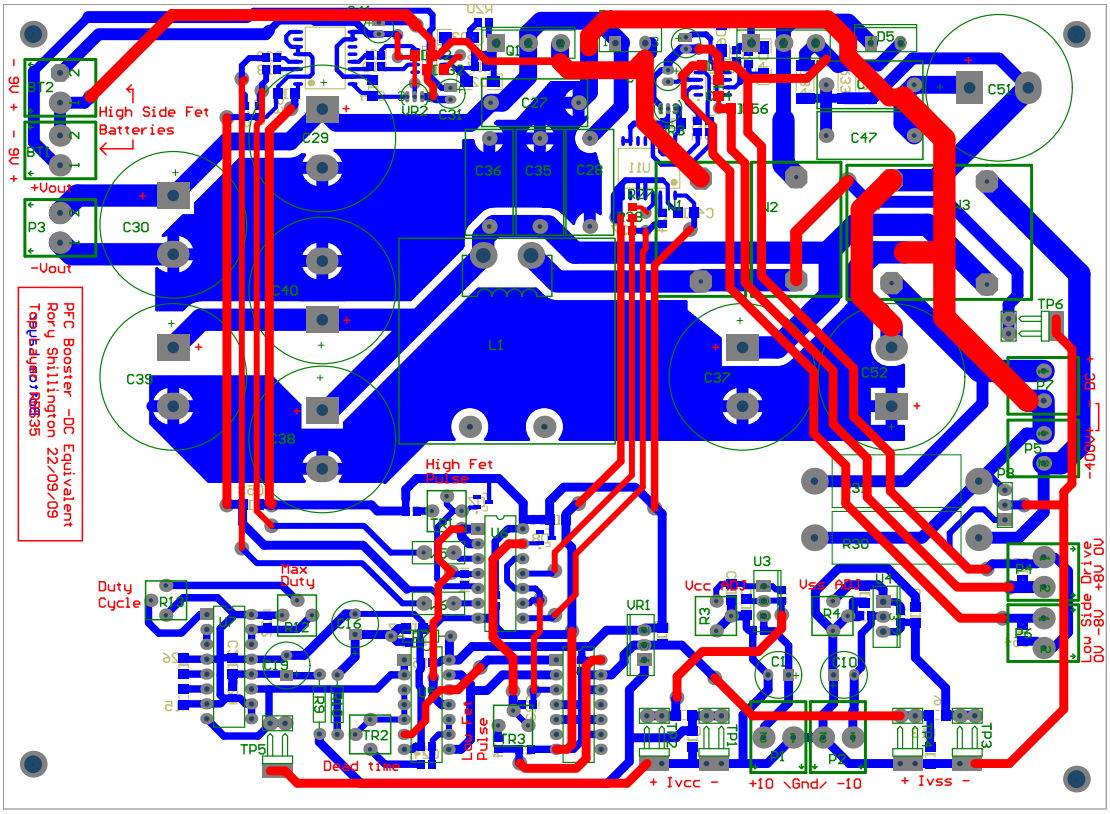


Figure 7-5: PCB layout for the PFC DC equivalent prototype

7.7.1 High voltage decoupling

The DC voltage source simulating the mains input to the PFC was heavily decoupled to minimize its AC impedance. The 400V voltage source simulating C2's charge in Figure 6-2 has extremely rapidly changing currents drawn from it, so high frequency decoupling was provided across it, as physically close to transistor Q2 as possible, by polyester capacitors. Electrolytic capacitors were located nearby to provide bulk decoupling.

When choosing the exact location of capacitors, the return current paths were carefully considered to ensure that the capacitors provide decoupling in close physical proximity to where it is needed and decouple relative to the correct nodes.

7.7.2 High current loop minimization

To achieve high switching speeds and low emissions, traces carrying the most rapidly changing currents were routed with the highest priority to allow their length to be optimally reduced. Further traces were then routed in order of decreasing $\frac{di}{dt}$. When the

traces being routed were return paths for other traces, loop area was minimized, albeit at the expense of trace length, by running return traces over their companion traces, wherever possible, on the other PCB layer.

7.7.3 Low voltage circuitry

Low voltage circuits were located some distance away from the high voltage switching circuitry because of the large physical size of the high voltage passive components, and to avoid interference from the high voltage circuits. The location of low voltage circuits also improved laboratory safety when adjusting dead time, duty cycle and pulse-shaping characteristics.

7.8 Conclusions

In this chapter, the development of a prototype circuit was presented for the DC equivalent of the PFC boost converter described in Chapter 6. The circuit implementation details were described to demonstrate some of the issues that are typically faced when designing circuits with EM SiC JFETs.

In Chapter 8, the performance of this prototype is measured and compared to the performance predictions that were presented in Chapter 6 to evaluate their applicability.

Chapter 8 PFC Prototype Testing

8.1 Introduction

In this chapter, the prototype PFC DC equivalent circuit presented in Chapter 7 is tested. The development of a control circuit for the PFC is described as well as the measurement techniques used for the performance evaluation. Comparisons are then made between the measured performance of the prototype circuit and the mathematical predictions that were made in Chapter 6. Several challenges faced in this chapter are also described as well as the opportunities for future work that they create, particularly around the control scheme.

8.2 Construction

The practical implementation of the DC equivalent circuit for the novel PFC topology is shown in Figure 8-1, constructed on a two layer printed circuit board using the artwork in Figure 7-5. Wire loops for current measurements are kept as small as possible, allowing just sufficient room for the jaws of a current transducer to close around them (top right above the pair of large electrolytic capacitors. Because of challenges with the destruction of transistors under some circumstances during testing, terminals were retrofitted for the power devices to assist changing of devices. These added approximately 4mm to the conductor length per pin, contributing an estimated 4nH of inductance. This is expected to slightly reduce the achievable slew rates and increase parasitic ringing on the gate of the SiC JFETs. The large negative gate voltage (-9V) being applied at turn-off is expected to prevent these parasitics from causing any false triggering or shoot-through.

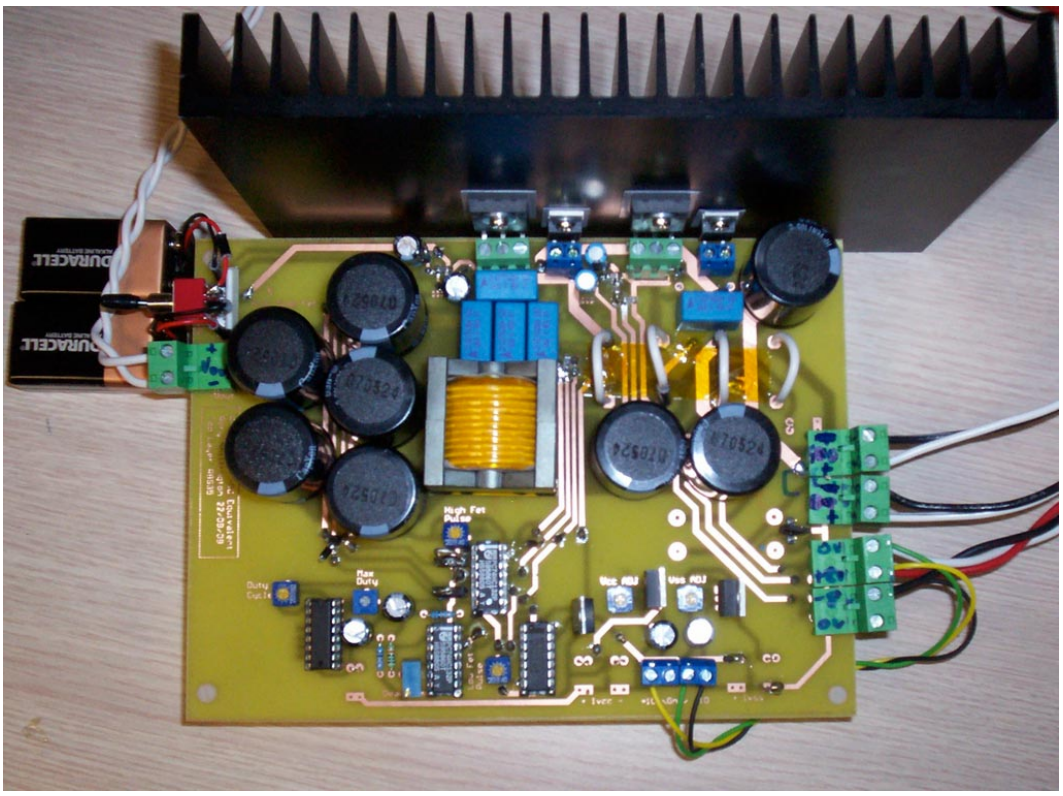


Figure 8-1: The assembled PFC DC equivalent circuit prototype

8.3 Operational Testing

8.3.1 Basic operation

Initially, the low voltage circuitry alone is powered up to confirm basic operation. The four logic signals generated are shown in Figure 8-2. Channel 1 shows the PWM signal applied to the upper JFET while channel 2 shows the brief pulses applied to the upper JFET via a lower impedance network to ensure fast turn-on. Channel three is the signal for the lower JFET while channel four shows the brief pulses that ensure fast turn-on of the lower JFET. The pulses are both shown adjusted to approximately 160ns in length. The dead time between the upper and lower JFETs is visible as the gap between channel 3 going low (centre of image marked by a vertical orange dashed line) and channel 1 going high.

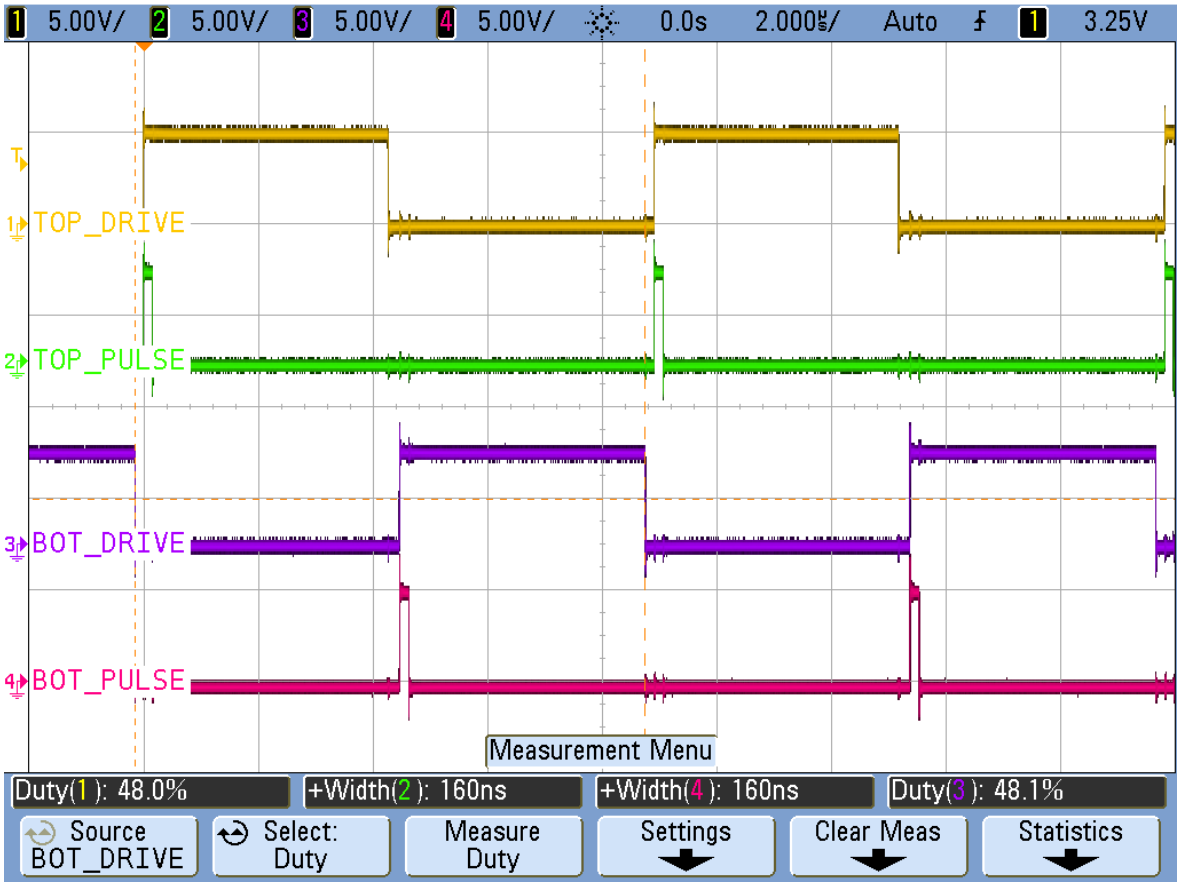


Figure 8-2: The four signals generated by the pulse-shaping circuitry

The drive circuits are powered up next and the gate-source voltages of the JFETs are observed. The dead times are adjusted to achieve a value that is as small as possible to maximise the time when transistors are conducting instead of diodes, but sufficiently large to ensure that shoot-through does not occur. Shoot-through is monitored for by observing the transistor currents with an oscilloscope during adjustment. The adjusted value was approximately 100ns. The adjustments are important because turn-on pulses that are too short result in slower rises in gate-source voltage. This leads to slower turn-on of the JFETs and excessive switching losses. Pulses that are too long can cause excessive gate-source overvoltage conditions which waste power and can potentially damage the JFETs.

The power stages are powered up by connecting a short circuit across the 400 volt C2 input, and a DC power supply to the mains input. Figure 8-3 shows the circuit operating with an output voltage of approximately 170V. The pink maths trace (10V/div) shows the upper JFET's gate-source voltage while trace three (purple) shows the lower JFET's gate-source voltage. Trace four (red) shows the voltage on the node between Q1 and Q2 relative to ground. The dead time is visible as the time when both the upper and lower JFETs have

a zero gate-source voltage. It can also be observed that Q1 is experiencing zero voltage switching because the bridge voltage is already at its peak (and hence the drain source voltage of Q1 is zero) when Q1 turns on and the bridge voltage remains at this level after Q1 turns off, freewheeling through diode D1. The visible noise occurs due to currents flowing in the circuit's ground planes resulting in a phenomenon referred to as ground bounce. The currents cause small voltage differences to occur between different points on the ground planes including the measurement ground points. Differential probes could have alleviated this problem; however, the bandwidths of the probes available were insufficient for these measurements.

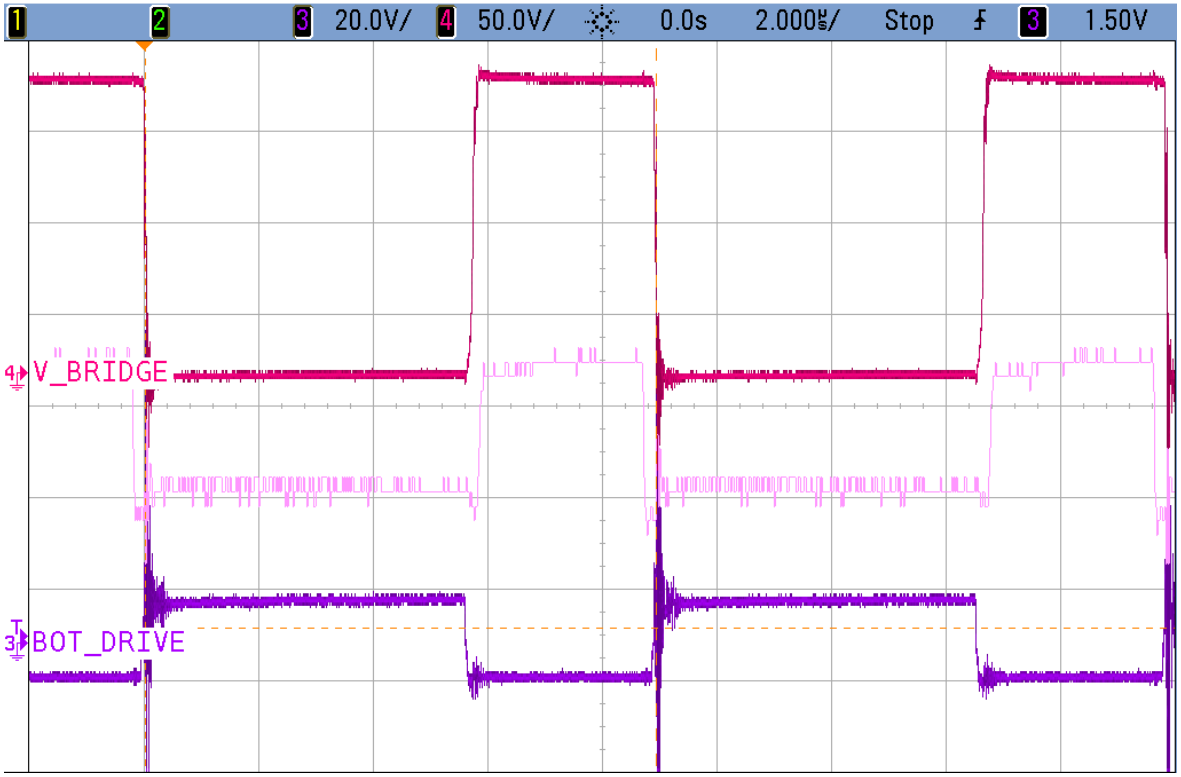


Figure 8-3: The PFC circuit operating with 50 volts on the mains input and zero volts across C2. Trace 3 (purple) is the lower JFET's gate-source voltage, the centre trace (pink) is the upper JFET's gate-source voltage and trace 4 (red) is the lower JFET's drain-source voltage.

8.3.2 Amendments

During early testing of the prototype, the lower JFET, Q2, was observed not always turning on at the appropriate time. Figure 8-4 shows the gate and source voltages of Q1 (trace one, yellow and trace two, green) as well as the gate and source voltages of Q2 (trace three, purple and trace four, pink), relative to ground. Under normal operation, the gate voltage of Q2 rises above its source voltage, causing the gate and source voltages of

Q1 to fall. However, during this time, the gate of Q1 remains below the source of Q1, maintaining Q1 in an off state. When Q2's gate voltage goes below its source voltage, the bridge voltage (and the gate and source voltages of Q1) rise while Q1's parallel diode D1 freewheels. After a short dead time, Q1 is turned on under ZVT by its gate voltage going above its source voltage. In Figure 8-4, a glitch is visible where the voltage between Q1 and Q2 rises abnormally. Q1 did not turn on because its gate voltage had already swung well below its source voltage and remained lower. Meanwhile, Q2 had an abnormally small gate source voltage that was neither positive enough to cause it to turn on nor negative enough to guarantee that it would remain off. This issue occurs sporadically and is accompanied by audible noise emitted by the inductor and excessive heat being dissipated by Q2.

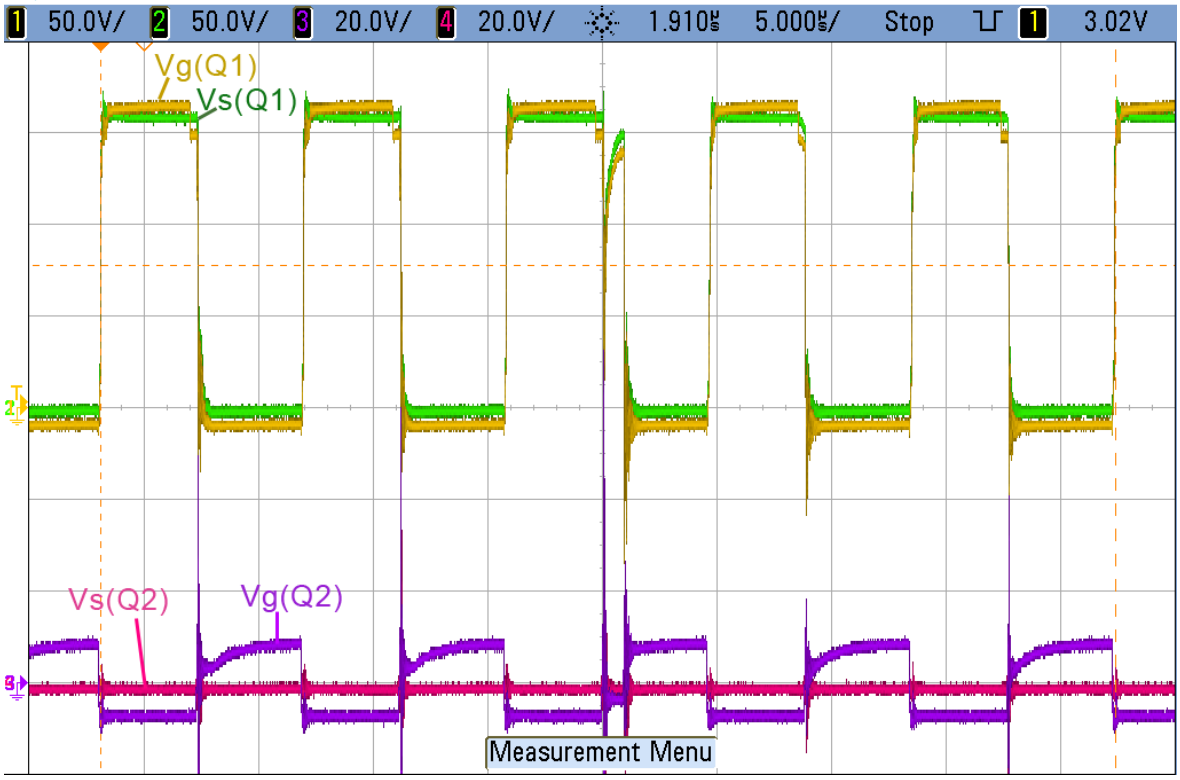


Figure 8-4: Q2 failing to turn on properly

A differential probe was used to observe the logic signals on the node between the isolator and the MOSFET driver, albeit with the bandwidth limitations of the probe. The problem did not occur when the differential probe was connected, indicating that the issue is as a result of termination in this part of the circuit. The issue was serendipitously cured by the parasitic coupling of the differential probe. In the original design, the isolator output and

MOSFET driver IC input were connected by a 1kΩ resistor. Changing this resistor to 22Ω and adding a pull-up resistor of 1kΩ solved the problem permanently.

Protection diodes were added to the JFET drive circuits as shown by Da and Db in Figure 8-5 for the high-side JFET. These diodes clamp the gate voltage for each JFET, preventing it from going far outside of the driver IC's supply rails. This provided an added level of protection against driver IC failure during fault conditions.

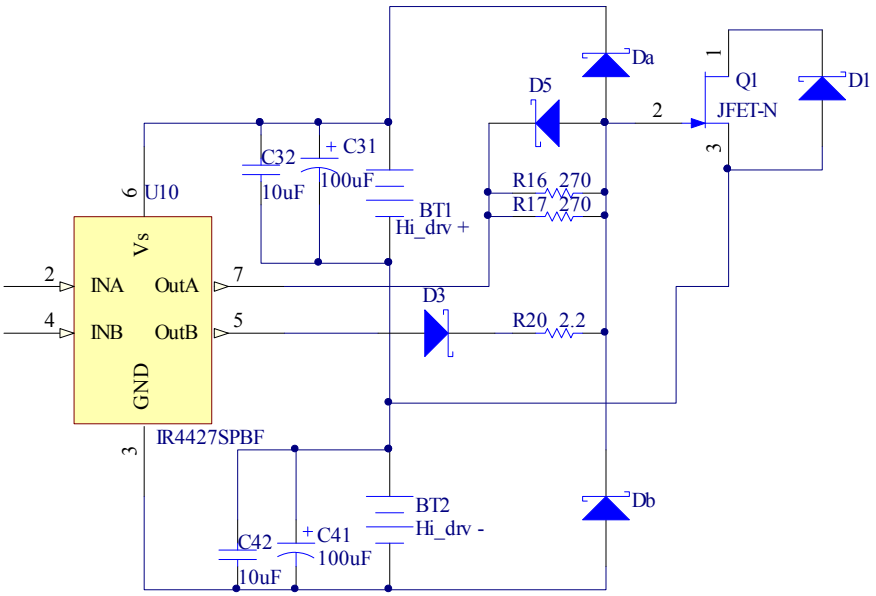


Figure 8-5: Diodes Da & Db protect MOSFET driver U10 from transients. (Diodes are similarly placed around Q2)

Another issue with the original prototype circuit is that the strategy of turning Q1 on when Q2 is off is not appropriate for discontinuous conduction mode. The current through the inductor falls to zero before Q1 turns off, causing the current to reverse polarity, briefly causing the transfer of energy from the output capacitor C1 to the mains. Disabling synchronous rectification solved this problem during initial testing, at the cost of a small decrease in efficiency caused by D1's forward voltage being larger than the voltage drop across Q1 when turned on for synchronous rectification. Under correct operation, the small efficiency improvement can be realised through the design of a more sophisticated control system for Q1.

8.3.3 Duty cycle feedback control

Operation of the revised DC equivalent prototype, with 400 volts applied to C2, allowed the open loop duty cycle to be manually adjusted to achieve an output voltage of approximately 400 volts. The need to adjust both the load resistance and the DC input voltage simultaneously makes open loop control of the duty cycle impractical and potentially dangerous. If the load becomes disconnected (as occurred during initial laboratory testing, due to failure of the load itself) the output voltage rises rapidly, resulting in destruction of the SiC JFETs.

To overcome this control and safety issue during prototyping, a simple feedback circuit was proposed. Because the DC prototype operates only at discrete points in the positive mains half-cycle, the feedback circuit does not need to react as quickly as needed in a full AC PFC circuit.

The converter's gain is highly non-linear. As the input voltage tends toward zero, the voltage gain tends to infinity. It is assumed that the JFETs are only driven when at least 1% of the maximum input voltage (3.25V) is applied to the prototype. Under these conditions, if the duty cycle is limited to a maximum of 95%, the voltage gain is capped at 40dB. Because the PWM circuit requires a change in error signal of 2V to achieve a zero to 100% duty cycle change, the converter's maximum plant gain is half of this value (34dB). Meanwhile, the minimum voltage gain to duty cycle ratio occurs at the DCM to CCM boundary where the gain of the converter is only 8dB with a plant gain of 2dB.

The proposed control circuit is shown in Figure 8-6. The output voltage of the converter is divided down by several resistors and noise filtered by C64. The output impedance at this point is very high due to the voltage divider so U8B is used as a buffer, provides a necessary inversion and creates some high frequency roll-off. U8A creates a Proportional-Integral (PI) characteristic with R39, R42, C60 and C61. To choose the component values for the PI controller, C60 and C61 were initially left out of circuit. R42 (the proportional term) was initially set to 150kΩ, to achieve a gain of 43.5dB. This was done to counteract the gains of the voltage divider and the plant gain at the DCM to CCM boundary (-45dB and 2dB respectively).

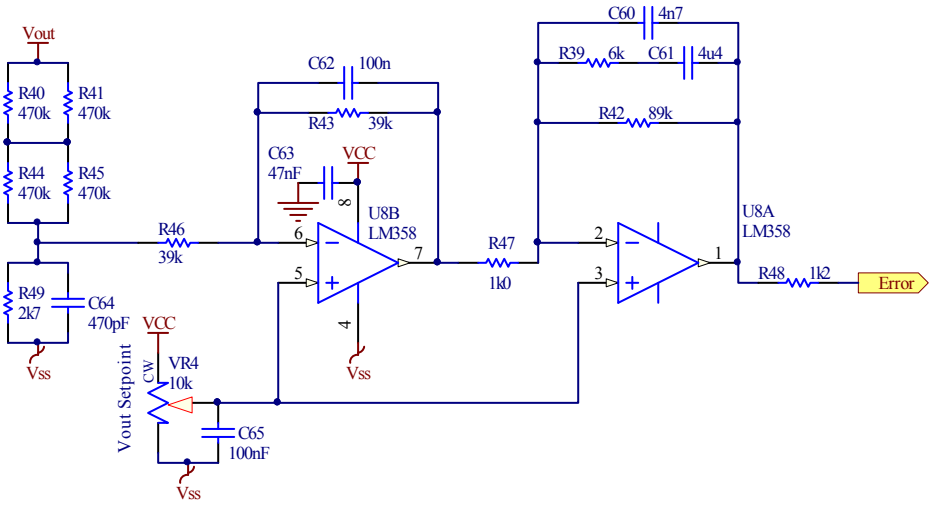


Figure 8-6: The proposed feedback network for the PFC prototype circuit

With this initial value, the converter was tested, initially at power levels of several hundred watts in discontinuous conduction mode. The proportional gain was found to be too high and adjusted down by hand. The integral term was then added and adjusted by trial and error in coordination with further adjustments to the proportional gain to minimise oscillations and offset error. The initial values used for the integral term were 22kΩ for R39 and 1µF for C61, with final values of 6kΩ and 4.4µF being used. The final value used for R42 was 89kΩ, giving a proportional gain of 39dB.

The value of 4.7nF, used for C60 was found to sufficiently attenuate the gain at high frequencies. A simulation of the circuit's AC response is shown in Figure 8-7. The system unity gain point occurs at 4.56kHz, where the feedback loop has a gain of −34dB. The phase margin at this point is 125.5°, guaranteeing ample stability as well as sufficient gain to allow the correct set-point to be met. The unity gain point of 4.56kHz is also well below the switching frequency of 140kHz.

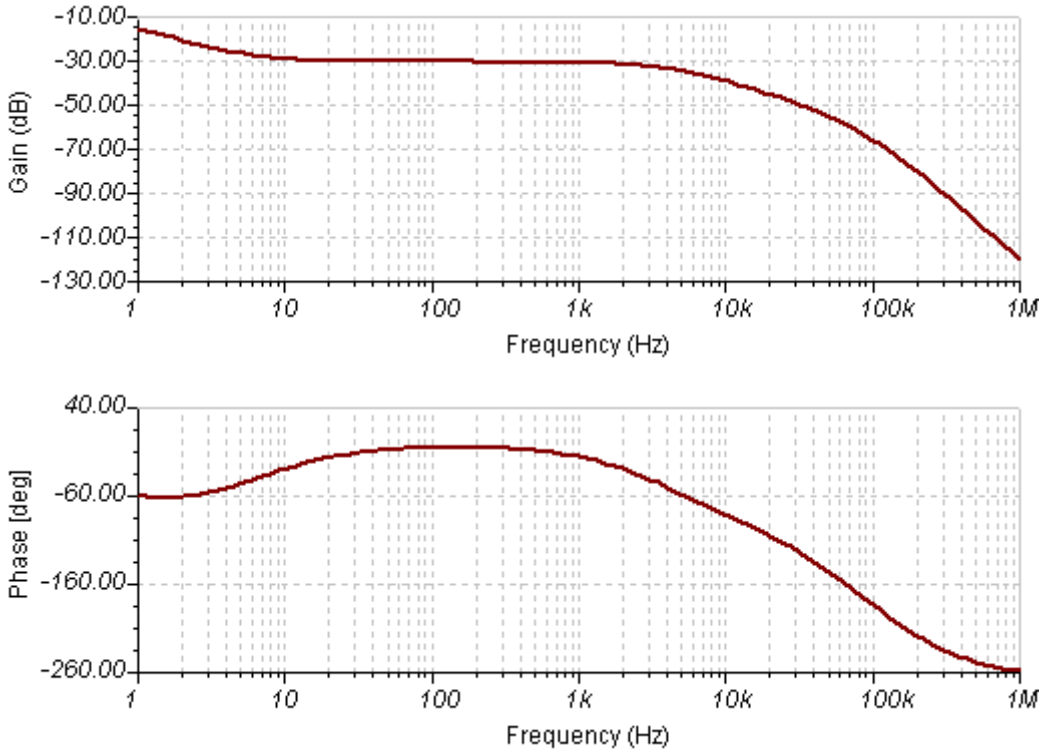


Figure 8-7: The AC response of the proposed feedback network

Because the converter exhibits such a broad range of plant gain over its operating range, it is recommended as a future improvement that the inclusion of a dynamic gain in the control loop be considered. The controller would need to decrease the gain of the control loop with increasing input voltage, particularly over the DCM range. This will allow the large loop gain required for small input voltages to be maintained without causing such severe oscillations at higher input voltages where the boost ratio and required loop gain are much smaller. Such a scheme would most probably be more easily implemented if the analogue control circuit was replaced with a digital controller.

In addition to the PI control circuit, a hysteretic over-voltage protection (OVP) circuit, Figure 8-8 was proposed to protect the system during PI controller tuning. The OVP circuit protects the converter from destruction by shutting down the PWM signal if the output voltage rises too high despite the actions of the PI controller. The OVP circuit has approximately 15V of hysteresis provided by R4. D2, R1 and C1 create an asymmetrical response which causes the circuit to respond faster to the start of an over-voltage condition than to its conclusion. LED1 provides a visual indication that the voltage is below the OVP threshold and extinguishes when an OVP condition occurs. This is used to assist the adjustment of R6 during OVP threshold calibration.

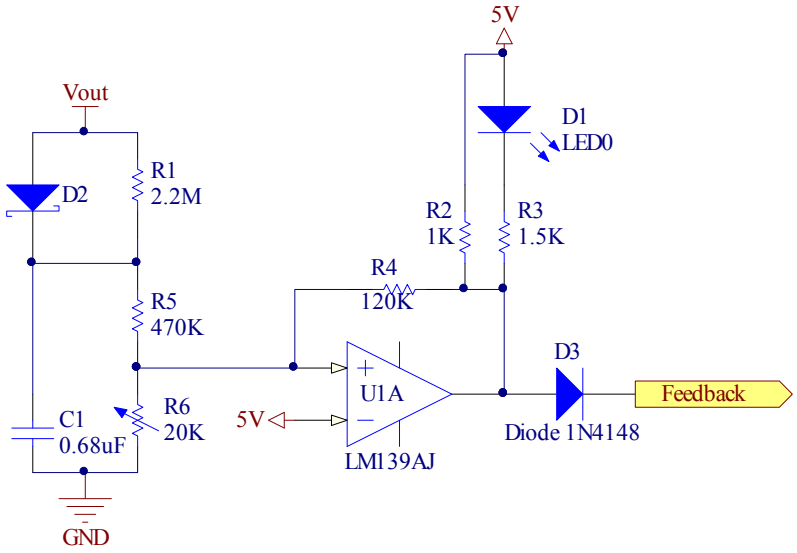


Figure 8-8: The over-voltage protection circuit

In addition to the PI and OVP circuits, a manual override switch is also implemented, allowing the PWM duty cycle to be disabled manually. C2 causes the circuit to ramp up slowly when the converter is first enabled. When the interlock is reset by briefly pressing switch S3, relay K1 is energised, forming a latch through diode D3. K1 disconnects C2 from the 5V rail, allowing C2 to discharge through R1 if switch S1 is in the enable position.

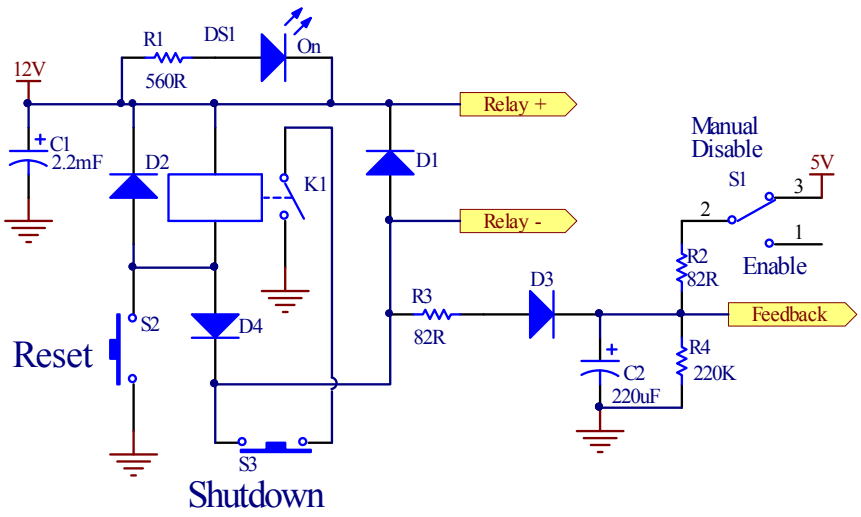


Figure 8-9: The interlock and manual control switch

Four other relays are driven by Relay+ and Relay-. These relays interrupt the supply of power to the equipment used to create the variable DC input and −400V supplies for the

converter prototype in the laboratory test setup. The control, interlock and over-voltage protection circuits are shown combined together in Appendix B, Schematic 6.

8.4 Test conditions

To operate the DC equivalent prototype, C2 needs to be supplied with up to 500W at −400V DC, while the mains input requires up to 4kW at the peak voltage of 325V. The output of the converter, meanwhile must be loaded at up to approximately 4kW at 400V DC.

To achieve this, C2 was powered from the DC bus of a large switch-mode power supply operating from an isolation transformer to allow the positive of the 400 volt bus to be grounded. The 'mains' DC input was generated by rectifying a three phase mains power source supply using large rectifier diodes and smoothing capacitors. The voltage was controlled by a three phase variac and isolation was provided by a three phase isolation transformer.

A test load was created by the combination of a switch-mode power supply to step the 400 volt DC output down to 48 volts and a 4kW 48V active load.

To measure the efficiency of the prototype converter, a Voltech PM3000A three phase power meter was utilized. The power meter has three channels that are each able to independently measure real power with a base accuracy of 0.05%. One channel is connected to the mains input of the converter, another to the C2 input and the last one to the DC output. To achieve accurate measurements, the circuit was first allowed to settle and reach thermal equilibrium at the particular operating point. The displays of the power meter were then frozen to allow a simultaneous reading of each channel to be recorded.

To ensure that the measurements were as accurate as possible, four wires were used to connect each channel to the point at which measurements are being made: two wires form a current loop through the PM3000A's internal current measuring precision shunt, while another two wires allowed the voltage to be sensed at the prototype PCB, avoiding cable losses in the current loops from introducing errors to the measurements.

8.5 Results

8.5.1 Operating points

To achieve unity power factor, the current drawn by the circuit is kept in proportion with the input voltage and the resulting power converted is proportional to the square of the input voltage. At full load from a nominal mains voltage of 230V, the average power level is 2kW so the converter experiences a peak power draw of 4kW at the 325V peak of each mains half-cycle. To establish the system efficiency over an entire mains cycle at a nominal power level, a number of discrete operating points were chosen over a mains quarter-cycle. By symmetry, these points are representative of an entire mains cycle. To allow the average efficiency to be calculated without having to weight the points, they were spaced evenly over the mains quarter-cycle based on energy transfer. At an average power level of 2kW, the energy transferred during a 5ms mains quarter-cycle is 10J so spacing the points 1J apart resulted in the points summarized in Table 8-1.

Time (ms)	V_{in} (V)	P_{in} (W)	Cumulative energy (J)
1.59	155.4	914	0.50
2.33	217.4	1790	1.50
2.81	251.1	2389	2.50
3.19	274.0	2844	3.50
3.52	290.7	3199	4.50
3.82	303.0	3477	5.50
4.10	312.1	3690	6.50
4.37	318.6	3844	7.50
4.62	322.7	3944	8.50
4.87	324.7	3994	9.50

Table 8-1: The 10 discrete test points spread by energy over a mains quarter-cycle

The results presented in this section follow this convention, with efficiency graphs showing the **instantaneous** voltages that the DC equivalent circuit uses to simulate points along the mains waveform in the x-axis for a nominal RMS mains input voltage of 230V. The voltages do not represent differing RMS mains voltages.

8.5.2 Measurements made

Since the points of interest for the efficiency calculation start at a reasonably high voltage, additional data were collected every 20V up to the first target point of 155.4V for the purposes of gauging the circuit's performance near zero crossings.

Below approximately 160 volts, the circuit always operates in discontinuous conduction mode. Under this mode of operation, significant ringing occurs after the current reaches zero because of the high quality factor of the inductor, as shown in Figure 8-10. The resonant frequency is approximately 600kHz, determined primarily by the inductance of the inductor and the parasitic capacitances of the transistors.

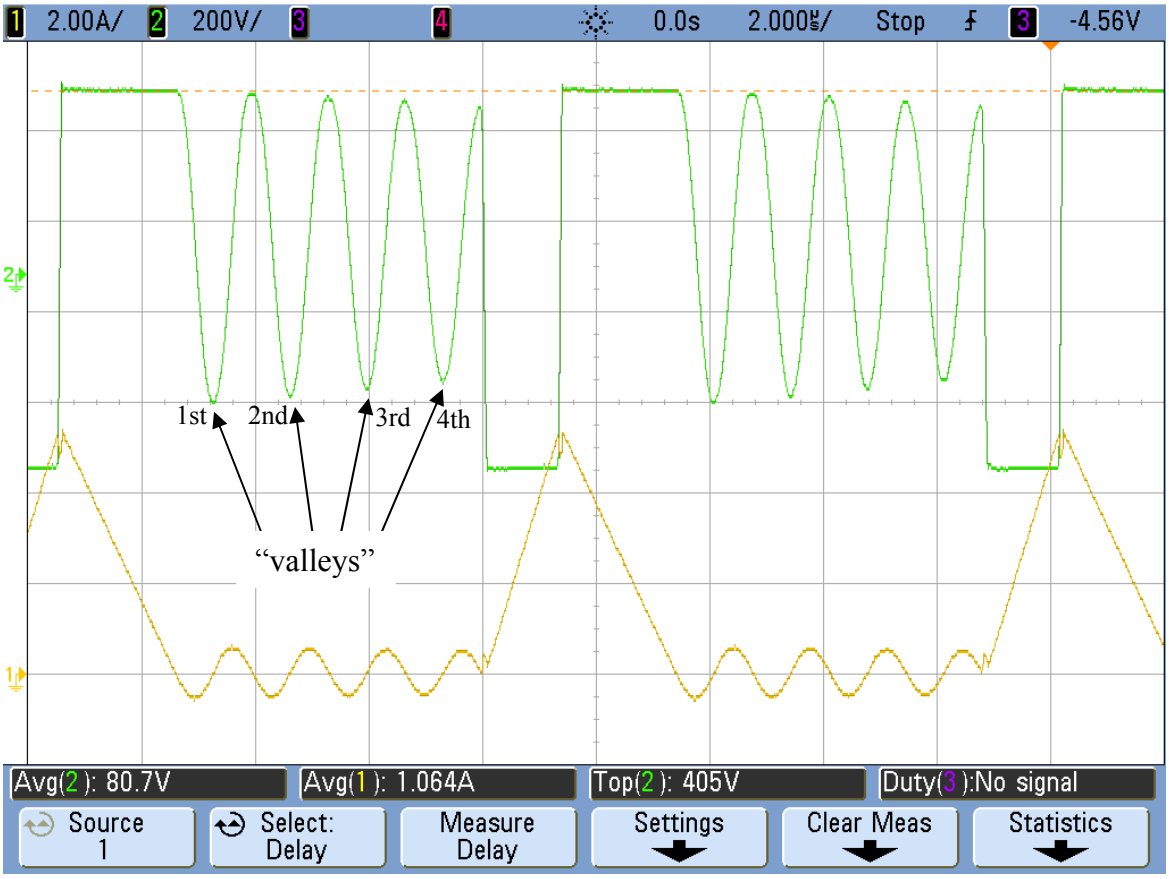


Figure 8-10: Ringing occurs when operating in discontinuous conduction mode. Trace 1 (yellow) shows the inductor current and trace 2 (green) shows the voltage on the L1, Q1, Q2 node.

As the input voltage and load power were changed, the feedback circuit adjusted the duty cycle to maintain a constant output voltage. This varied the duration of the ringing and caused variations in the instantaneous voltage appearing across Q2 at its moment of switch-on. The feedback circuit was able to keep the output voltage and voltage across Q2

relatively stable under most operating conditions. However, when the bridge voltage at the time of Q2's turn-on was near a local minimum or "valley", the feedback circuit struggled to repetitively achieve turn-on of Q2 near the bottom of the valley, instead hunting around it. This interaction between the control loop and the circuit resonance caused the peak current from one cycle to another to vary significantly as shown in Figure 8-11.

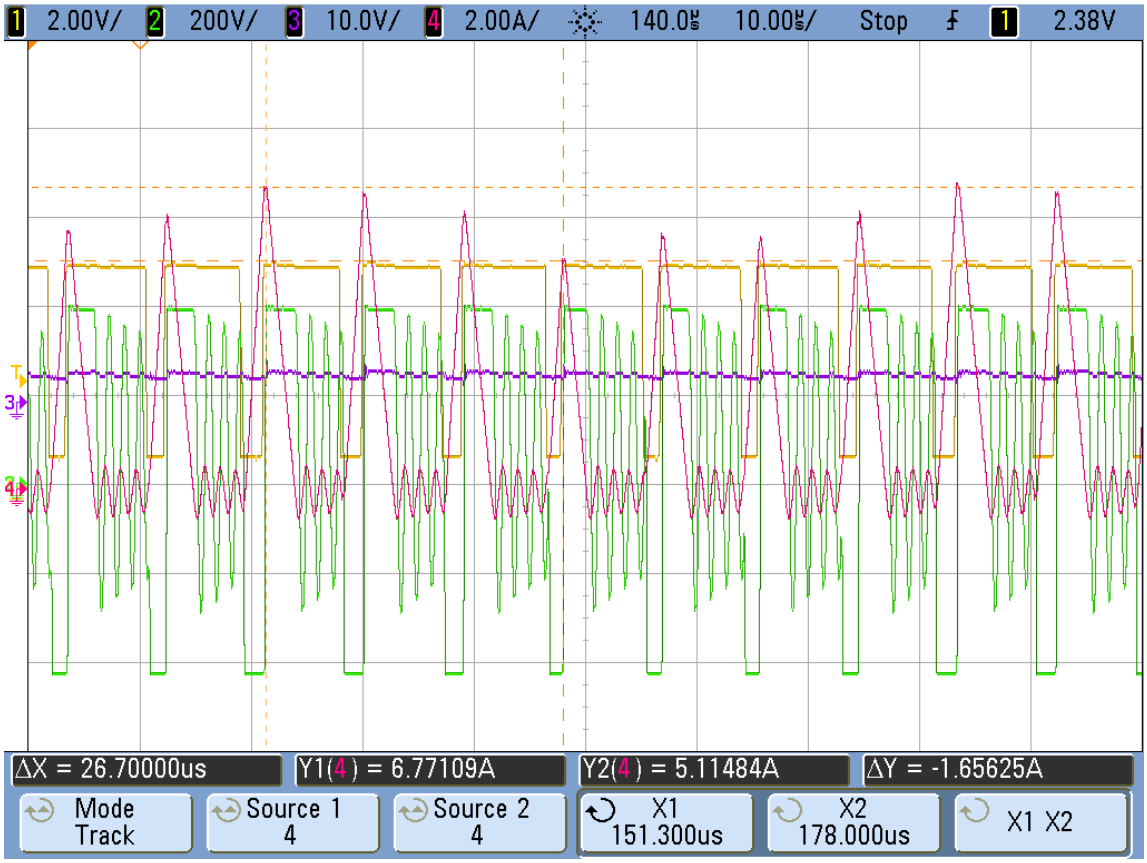


Figure 8-11: The peaks of the inductor current (channel 4, pink) vary due to interactions between circuit resonance and switching frequency. The drain voltage of Q2 is shown on channel 2 (green), the (inverted) PWM signal on channel 1 (yellow) and the output voltage feedback signal on channel 3 (purple).

The interaction is self amplifying: if turn-on of Q2 occurs slightly before a valley, resonant current through the inductor has a positive polarity and rises to a larger peak value during the fixed on-time. It then takes longer for the current to decay to zero and begins ringing later, resulting in the next turn-on time occurring earlier in the ring sequence (and thus further ahead of the valley). Conversely, if turn-on of Q2 occurs slightly after a valley, resonant current through the inductor at that moment is negative, resulting in a lower peak current being reached at the end of Q2's on time and a sooner commencement of ringing,

leading to Q2's next turn-on occurring later in the resonant sequence (and thus further after the valley).

This effect caused the operating point of the converter to diverge away from a nearby valley until the feedback circuit exerted sufficient correcting force to push it back, after which the integrator would begin to integrate out the stale past errors, allowing another divergence away from the valley. As the input voltage and output load were varied, the converter would eventually pass through a valley and begin diverging away from it in the other direction. Significant variations in peak current from one cycle to the next occurred because of this phenomenon when operating close to a valley such as in Figure 8-11 whereas operation near 'peaks' (local maxima) such as in Figure 8-10 were very stable and exhibited minimal variation in peak current from one cycle to the next because the tendency was to converge on these.

Another observation made was that the severity of the hunting around each valley became worse with decreasing numbers of valleys i.e. divergence away from the 3rd valley was stronger and caused more variation in peak current than the divergence away from the 4th valley. As the turn-on of Q2 was brought near to the 1st valley (critical conduction mode) the hunting became extremely large and consistently resulted in the destruction of the transistors. It is likely that the cause of the destruction was the peak current reaching unacceptably large magnitudes in excess of those predicted under steady state conditions because a relatively small divergence away from the valley into continuous conduction mode could result in a significant increase in average current. Further increases in input voltage and output power could have been achieved with a more advanced peak current sensing control scheme to properly dampen the hunting of the control circuit around the each valley of the resonance.

Increasing the inductance would shift the discontinuous/continuous conduction boundary to a lower voltage but does not solve the control problem because discontinuous conduction will still occur near the zero crossing unless the inductance is unreasonably large or crossover distortion is permitted. A significantly larger inductance would also decrease the circuit's ability to react quickly to changes in load. Decreasing the circuit inductance would shift the discontinuous/continuous conduction boundary to a higher voltage, potentially allowing for discontinuous operation up to full power at the maximum

input voltage. Although this avoids the control issue, the current ripple on the input would likely be too high for power quality requirements. Either change to the inductor would also violate the commercial constraints on inductor selection outlined in section 6.1.

The measurements obtained below the unstable threshold are summarized in Table 8-2. The measurements were conducted as close to the full load curve as possible. Actual positions of the measurements ranged from 97.4% to 100.0% rated load.

Vin (V)	Pin (W)	P_{400V} (W)	Pout (W)	Circuit Efficiency	System Efficiency
50.54	95.56	350.8	427.6	95.80%	80.37%
60.37	134.46	402.9	513	95.47%	81.88%
70.14	186.31	460.1	628.8	97.28%	90.55%
80.74	246.3	510.7	736.1	97.24%	91.51%
90.46	307.5	555.4	831.6	96.37%	89.82%
105.5	417.3	608.7	1003.3	97.79%	94.56%
110.0	457.4	629.5	1062.9	97.79%	94.75%
114.9	497.6	646.5	1115.8	97.53%	94.31%

Table 8-2: Efficiency measurements at full load

As described fully in 6.3, power transferred from C2 to C1 in the AC PFC circuit is simulated by power transferred from V_{C2} to the load in the DC equivalent circuit. In Table 8-2 the 'system efficiency' takes this into account by only comparing the losses to the component of power transfer that goes from the mains to the load and excludes the capacitor to capacitor component of power conversion. The 'circuit efficiency' is the simple efficiency of the DC equivalent circuit, calculated by comparing the losses to the overall power converted by the circuit.

Additional measurements were made over a wider input voltage range within 15% of the half load curve. These measurements are summarized in Table 8-3 with the same circuit and system efficiency calculations as those in Table 8-2.

Vin (W)	Pin (W)	P_{400V} (W)	Pout (W)	Circuit Efficiency	System Efficiency	Load
90.0	186.47	346.3	505.4	94.86%	85.32%	60.79%
100.0	203.2	330.3	505.2	94.70%	86.07%	53.66%
110.6	219.4	311.8	506.2	95.29%	88.61%	47.36%
118.7	343.6	435.6	753.3	96.68%	92.46%	64.40%
119.8	235.5	294.5	505.9	95.45%	89.77%	43.33%
128.9	248.5	281.2	505.8	95.49%	90.38%	39.49%
139.75	383.8	377.9	739.2	97.05%	94.14%	51.89%
149.3	467.1	418.7	852.8	96.27%	92.94%	55.33%
158.4	549.4	442.0	966.2	97.46%	95.41%	57.81%

Table 8-3: Additional PFC prototype efficiency measurements taken at partial loads

The locations of all the operating points at which efficiency measurements were taken in Table 8-2 and Table 8-3 are shown in Figure 8-12. Full and half power curves are also shown which follow the trajectories in *Eq 8-29* and *Eq 8-30*, based on average power levels of 1kW and 2kW respectively.

$$P_{half} = \frac{V_{in}^2}{325^2} \cdot 2000 \qquad \textit{Eq 8-29}$$

$$P_{full} = \frac{V_{in}^2}{325^2} \cdot 4000 \qquad \textit{Eq 8-30}$$

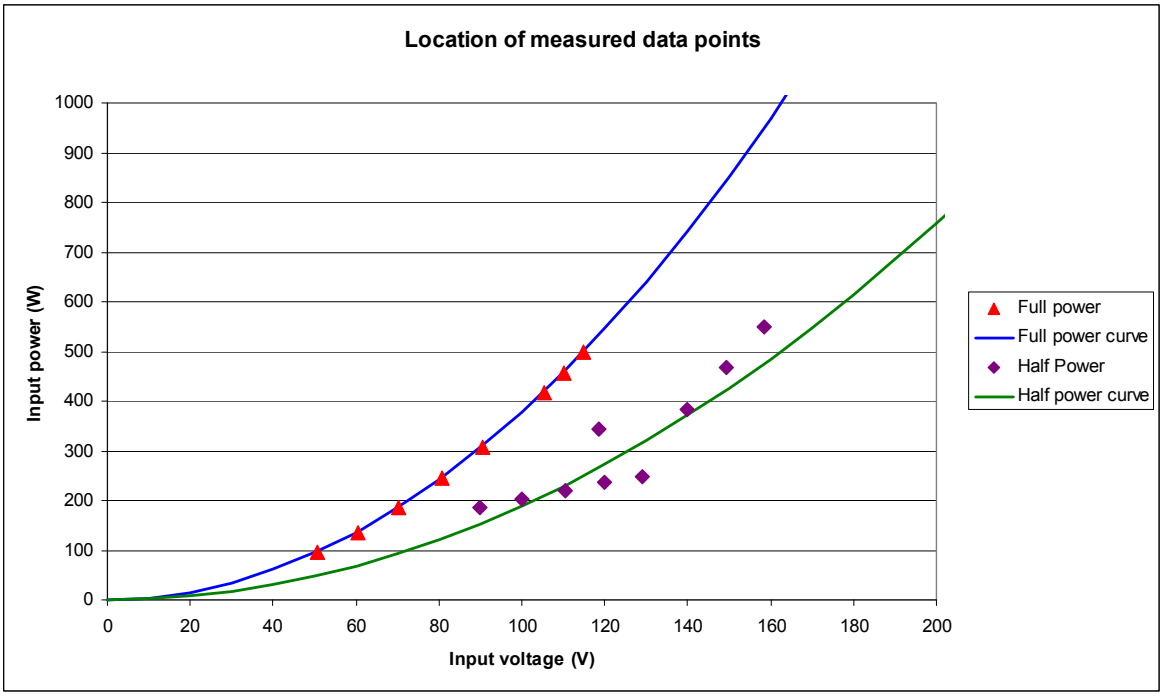


Figure 8-12: Locations of the instantaneous operating points at which efficiency measurements were made, relative to the full and half load curves

The curves follow the sine-squared voltage to power relationship resulting from the linear current to voltage relationship described in section 6.2.1 that is necessary for unity power factor operation. The graph in Figure 8-12 shows the alignment of the measured data points with the trajectories of the PFC in its real world application. It was not possible to obtain data points above 550W input power with the prototype circuit.

From the data gathered, the efficiency at full load is shown graphically in Figure 8-13 along with measurements that were within 15% of half load. These measurements provide insight into the performance of the PFC at low input voltages near the zero crossing points of the mains.

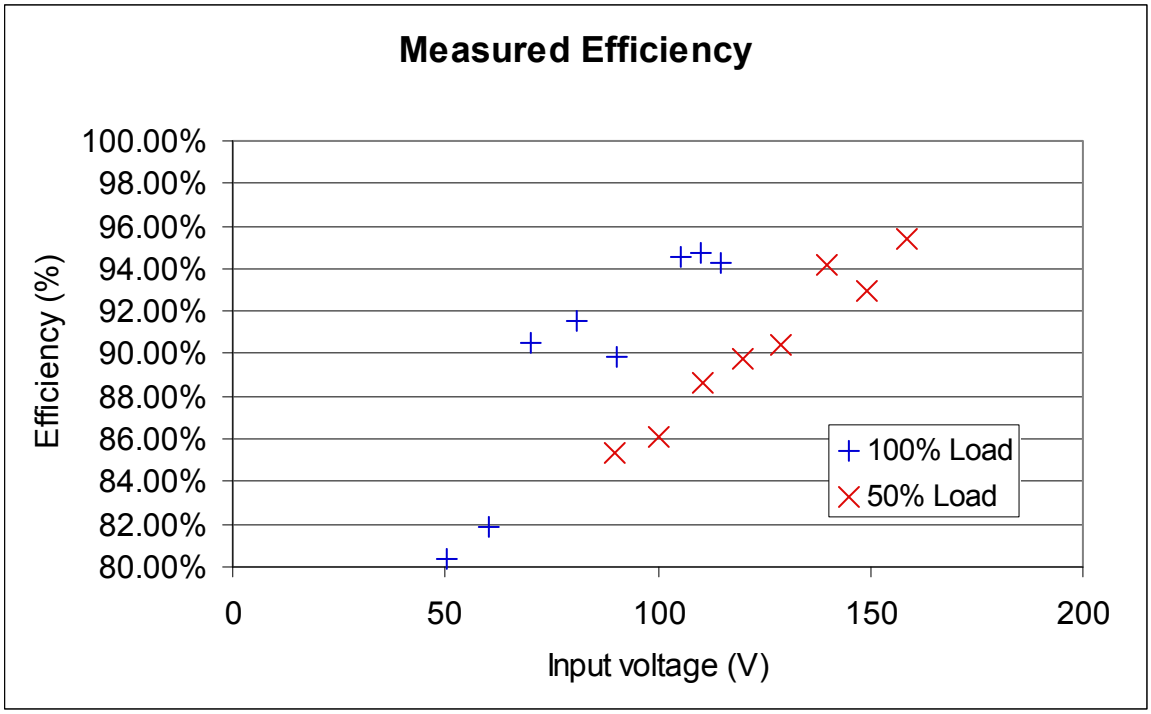


Figure 8-13: The efficiency measurements shown graphically at full load and half load at several instantaneous points on the mains waveform

The oscillatory variation on the efficiency curves is due to the variations in the voltage across Q2 that were present at the moments of switch-on. The local peaks in efficiency represent Q2 turning on with a minimal voltage across it, while the troughs represent Q2 turning on with close to the full 800V of the two capacitors appearing across its channel.

8.5.3 Comparison with circuit model

Figure 8-14 shows the measured results for a full 2kW load compared to the modelled circuit performance. The measured data points all lie between the best and worst case models. The measured results are within 4.2% of the average of the best and worst case models.

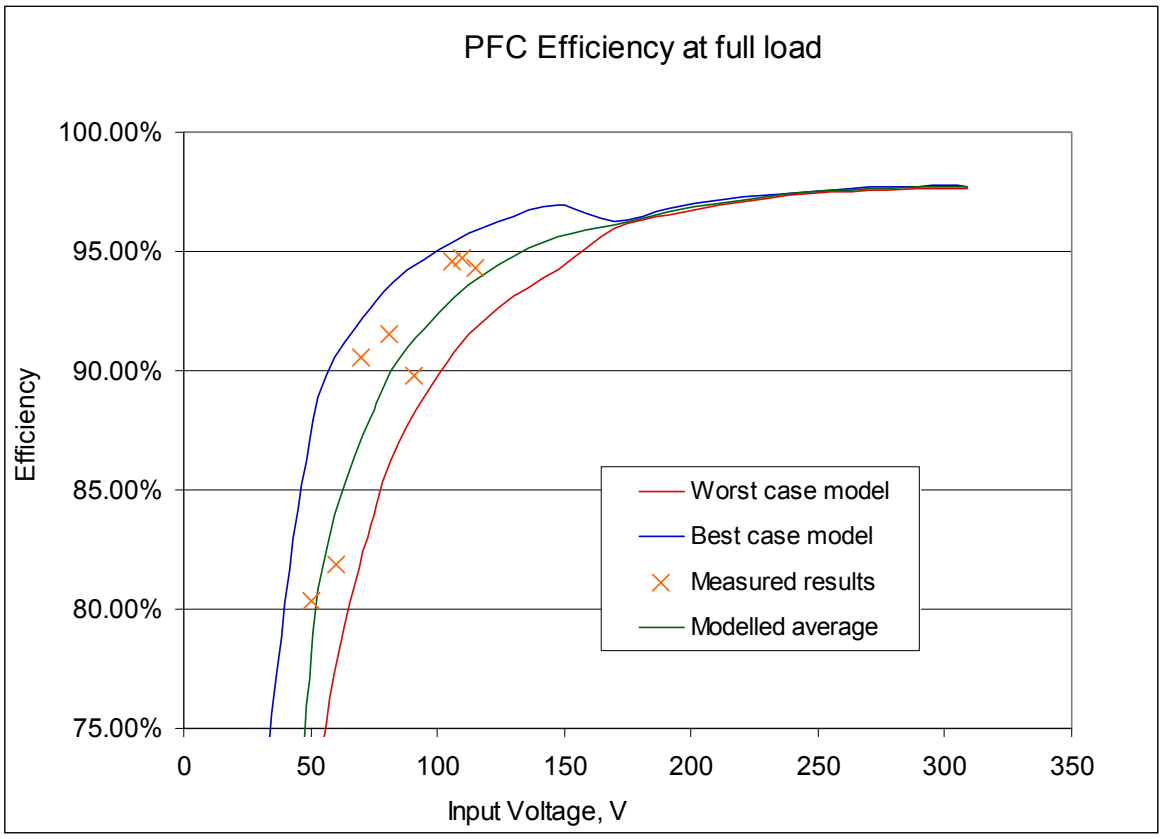


Figure 8-14: The measured efficiency against instantaneous voltage points on the mains waveform at full load, closely following the modelled efficiency

The model was also recalculated for a 50% load (equivalent to a 1kW PFC). The results are shown in Figure 8-15 along with the measured data from Table 8-3. As with the measurements conducted at full load, the half load measurements lie between the best and worst case models and within 3.5% of the average of the two models. It was also noted that the measured half-load data points lie closer to the worst case model than the best case model. This suggests that the model overestimates the degree to which losses increase with load. A model that is more optimistic about conduction losses and pessimistic about switching losses might better predict the performance of the PFC circuit over a wide operating range.

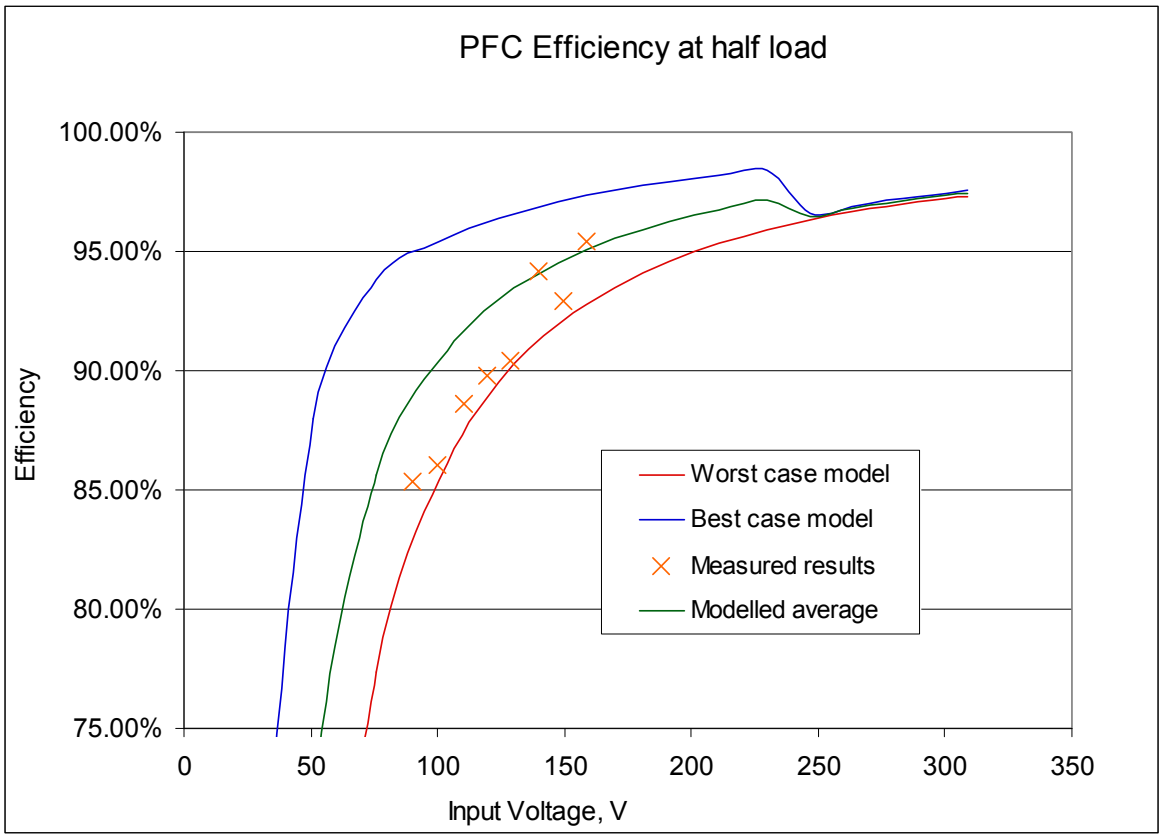


Figure 8-15: Measured and modelled efficiency against instantaneous points on the mains waveform at half load (1kW average)

Reducing the input voltage will only shift the discontinuous/continuous conduction boundary to a lower voltage because the duty cycle will have to increase to compensate for a larger boost ratio. The deviation from a 230V RMS input voltage curve also detracts from the real-world applicability of a the AC version of the PFC circuit.

8.6 Summary and conclusions

A prototype for the PFC circuit modelled in Chapter 6 and designed in Chapter 7 was constructed and tested. With the addition of a feedback circuit to automatically adjust the duty cycle, the PFC circuit operated at power levels up to 1kW. Soft turn-on was observed during discontinuous conduction where under certain loading conditions, the JFETs turned on with less than 800V across them. These operating regions correlated with peaks in electrical efficiency. The measured efficiency in discontinuous conduction mode varied due to the different degrees of soft switching, within the bounds of the best and worst case models from Chapter 6 for full load. At half-load, the efficiency was slightly lower than the average prediction, but also remained within the bounds of the best and worst case

models. When the average of the best and worst case models was calculated, the measured data points lay within 4% of the average prediction at full load and 5% at half load. Limitations in the physical prototype circuit's ability to operate in continuous conduction mode prevented data from being collected over a sufficiently wide range of operating conditions to verify the predicted efficiency range.

The efficiency of the proposed PFC circuit is high, but does not rival that of the best PFC circuits which can achieve more than 98% efficiency despite using two series conducting semiconductor devices. This is due to the transistors in the proposed PFC circuit having to swing 800V compared to the 400V swing experienced by transistors in most other topologies. The increase in switching losses due to the larger voltage swing outweighs the saving in conduction losses that is achieved by only having one semiconductor device conducting at any time. The switching losses comprise a combination of stored energy in the output capacitance and the occurrence of non zero-voltage switching.

If the switching frequency was varied with load such that Q2 was always turned on during a resonant 'valley' where its channel voltage was at a local minimum, turn-on losses would be minimized. The predictions in Table 6-4 based on the model in Chapter 6 suggest that the difference in turn-on loss for Q2 turning on at a peak compared to a valley during discontinuous conduction mode is 3.92W. The main trade-off of performing valley switching is that the switching frequency will vary. This is not a problem, but has ramifications for control loop and EMI filter design.

By incorporating a capacitor in parallel with Q2, it would be possible to achieve close to ZVT turn-off transitions, thus minimising turn-off losses. This technique has the disadvantage of increasing the turn-on losses during continuous conduction mode because the charged capacitor appears across Q2 during turn-on. This can be mitigated by switching the capacitor in and out of the circuit during discontinuous and continuous conduction modes with an auxiliary switch, but the added cost and complexity have to be weighed up against the efficiency benefits.

Chapter 9 SiC JFETs in a commercial telco rectifier

9.1 Overview

A recent commercial product, manufactured by Eaton Corporation is the APR48-ES energy saver rectifier. This product was chosen as a test platform for testing SiC JFETs as potential drop-in replacements for silicon MOSFETs in a real-world application.

9.1.1 Transistors and test platforms

In this chapter, two separate physical APR48-ES rectifiers are used for testing: a pre-production engineering prototype and a final production version. The pre-production rectifier was initially used to test the EM SiC JFETs that were available early in the research period. Later, a new EM SiC JFET became available, after the original pre-production rectifier had been inadvertently disposed of. A production APR48-ES rectifier, available at the time was used for testing the new EM SiC JFETs.

This Chapter introduces the SJEP120R063 and SJEP120R100, two normally off SiC JFETs manufactured by SemiSouth that became available at different times during the research. The SJEP120R063 consists of two SJEP120R125 dice co-packaged in a single TO-247 case. The SJEP120R063 offers a two-fold reduction in $R_{DS(on)}$ compared to the SJEP120R125 but also exhibits parasitic capacitances more than twice as large and can suffer from ringing due to the two transistors sharing the same physical package leads. The SJEP120R100 is an improved single die EM SiC JFET introduced near the end of the research to supersede the SJEP120R125. The SJEP120R100 has similar characteristics to the SJEP120R125 with the main exception being a 20% lower $R_{DS(on)}$.

9.1.2 APR48-ES

The APR48-ES rectifier operates from an AC utility supply and delivers a 48V DC output suitable for telecommunications equipment at a load of up to 2kW. It achieves a conversion efficiency above 96% and a power density of 1.3Wcm^{-3} [127].

Both the pre-production and production APR48-ES rectifiers consist of a boost converter for active input power factor correction and an isolated resonant converter for output voltage regulation. The topology of the boost converter is shown in Figure 9-1.

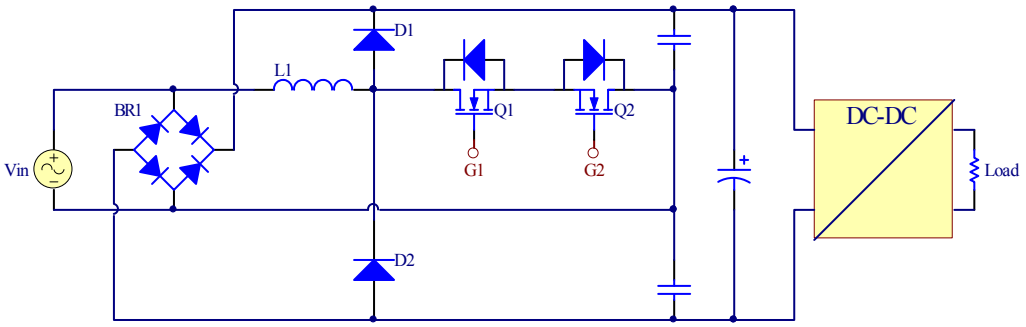


Figure 9-1: Boost converter topology for APR48-ES

During positive mains half-cycles, Q2 is turned on and PWM applied to Q1. When Q1 is on, inductor L1 is connected across the mains input, resulting in a rise in L1's current. Turning off Q1 then forces current to flow through L1, D1 and the bottom left diode in bridge rectifier BR1. By adjusting the duty cycle of PWM signal applied to Q1, the boost ratio can be adjusted to achieve unity power factor. During negative mains half-cycles, Q1 is left on and PWM is applied to Q2. D2 takes the place of D1 as "catch" diode, while a different diode in BR1 completes the circuit. Thus, at any time, only two semiconductor devices are conducting. During the on state, Q1 and Q2 conduct, whilst during the off state, D1 or D2 conducts as well as a diode in BR1. The implications of having two conducting semiconductors is a reduction in conduction losses of approximately a third compared to those of a classic bridge rectifier and boost converter combination. Switching losses are further reduced by the use of SiC Schottky diodes for D1 and D2. The diodes in BR1 do not need to be Schottky diodes because they only need to switch at 100Hz. If slow diodes are used, the bottom left diode in BR1 remains on during positive mains half cycles and the bottom right diode during negative half-cycles including during the periods of Q1 and Q2 being on with no current flowing through BR1. Litz wire is used in the winding of boost choke L1 to minimize skin effect, proximity effect and, as a result, high frequency copper losses.

9.2 Modifications to power converter

Figure 9-2 shows the gate drive network of a pre-production APR48-ES rectifier's boost converter circuit. Turn-on current flows via a 22Ω resistor, whilst turn-off current can also take an alternative path through a 4.7Ω resistor and diode, ensuring rapid turn-off times.

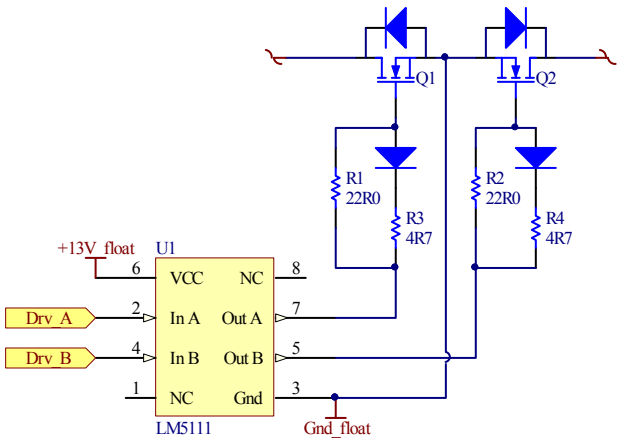


Figure 9-2: Gate drive circuit in the pre-production APR48-ES PFC boost circuit

To accommodate SiC JFETs in the boost converter, modifications were made to the gate drive network as shown in Figure 9-3. The LM5111 has a pull-up output resistance of approximately 30Ω and the SJEP120R125 JFET has a gate-source voltage drop of approximately 3V in the desired region of 50-100mA. R1 and R2 were chosen to limit the continuous gate current in each JFET to approximately 75mA. A more sophisticated drive circuit capable of delivering a negative output was not absolutely necessary because the topology does not contain a bridge and therefore does not exhibit significant shoot-through problems. The physical constraints of the commercial rectifier product were also such that modifications to use a bipolar gate drive would have affected the airflow, resulting in a different thermal equivalent circuit.

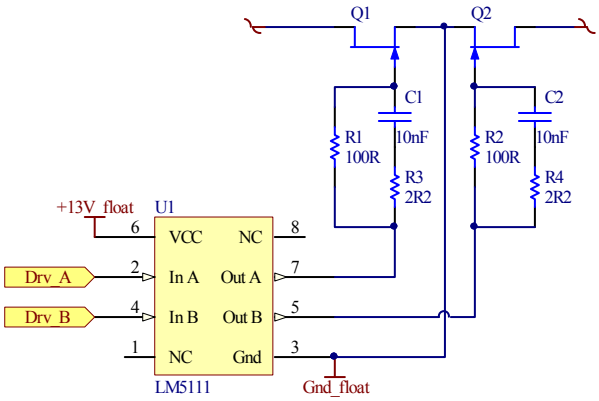


Figure 9-3: Modified gate network in pre-production APR48-ES to accommodate SiC JFETs

C1 and C2 provide a low impedance AC path as well as a charge-pump effect. The charge-pump effect increases the peak gate current to ensure rapid turn-on and pulls the gate-source voltage negative at turn-off to provide some immunity to false turn-on. R3 and R4

limit the peak gate current to dampen ringing. The value of 10nF for C1 and C2 was chosen using *Eq 9-31* from [103] where C_{BP} is the value of bypass capacitor C1 or C2.

$$\frac{2 \cdot Q_g}{V_{dd} - V_{gs}} \leq C_{BP} \leq \frac{4 \cdot Q_g}{V_{dd} - V_{gs}}$$
$$\frac{2 \cdot 30 \times 10^{-9}}{13 - 3} \leq C_{BP} \leq \frac{4 \cdot 30 \times 10^{-9}}{13 - 3} \qquad \textit{Eq 9-31}$$
$$6nF \leq C_{BP} \leq 12nF$$

9.3 Performance

9.3.1 Test methodology

A number of important aspects were considered during the design of the electrical efficiency measurement conditions to ensure a high level of accuracy. This is important because the differences between devices could be in the order of a few watts out of several hundred.

The power converter was supplied via a variac, allowing the input voltage to be controlled. At each operating point (load step), the variac was adjusted to compensate for droop before efficiency measurements were made, such that an input voltage of 230V RMS was maintained within a tolerance of 1V RMS for all data points.

The load on the output of the converter was adjusted in steps of approximately 100W. Output voltage was measured using a high precision Agilent 34970A data-logger. The output current was measured using a second channel of the Agilent 34970A, monitoring the voltage drop across a high precision, forced-air cooled DC shunt of known high accuracy. The input power was measured using a high precision, recently calibrated Yokogawa WT230 power meter.

The power meter and data-logger were controlled by a computer via a GPIB interface using a custom Python script. The scripts instructed the power meter and data-logger to simultaneously sample the input power, output voltage and output current. For each operating point, twenty samples were taken, synchronised to the same point in consecutive mains cycles (every 20ms) and averaged to reduce the impacts of transient noise. A settling

time elapsed at each operating point before data was acquired to allow a thermal equilibrium to be reached.

To minimize the differences in the testing platform for each set of transistors, the same physical telecommunications rectifier was used for every test.

9.3.2 Electrical efficiency

The electrical efficiency of the power converter with several different power devices is shown in Figure 9-4. Both 1200V SiC JFET devices offer electrical efficiency lower than that achieved by a 600V MOSFET (Infineon IPW6R099). The most appropriate 900V MOSFET (Infineon IPW9R120) exhibited poorer performance than the SJEP120R125 1200V SiC JFET but better than the pair of 1200V SiC JFETs copackaged in the SJEP120R063.

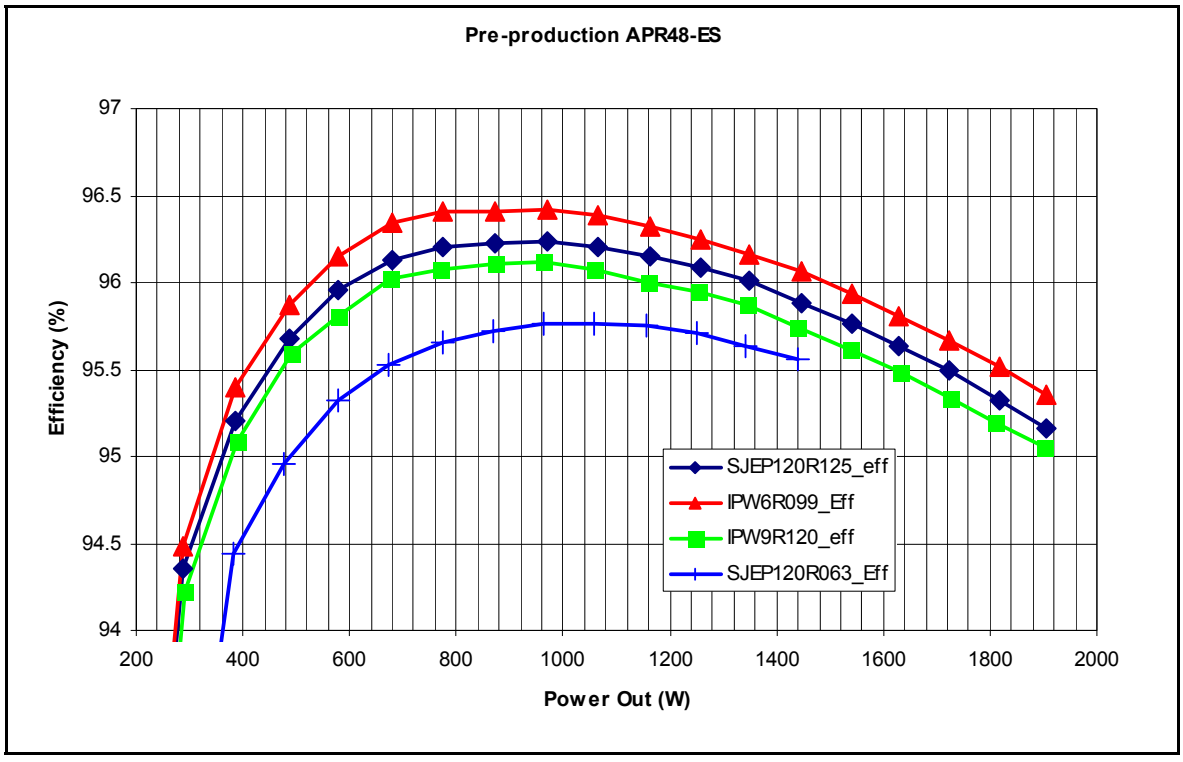


Figure 9-4: Electrical efficiency of the pre-production APR48-ES with different transistors in its active power factor correcting boost circuit

The 1200V SJEP120R125 SiC JFET achieves performance close to that of silicon MOSFETs that only offer half its blocking voltage. The superior performance of the SJEP120R125 1200V SiC JFET compared to the 900V Si MOSFET suggests that higher

voltage applications which do not permit the use of 600V Si MOSFETs may benefit from the use of SiC JFETs.

The particularly poor performance achieved by the SJEP120R063 suggests that although the positive temperature coefficient of the SJEP120R125 lends itself well to paralleling, doing so may not result in improved performance under all conditions. It is clear from Figure 9-4 that the efficiency of the pre-production APR48-ES rectifier with SJEP120R063 devices approaches that achieved with other switches as power increases, highlighting the improved conduction losses, however the improvements are overshadowed by other effects. In particular, it appears that the improvement in channel resistance was offset by the necessary increase in gate bias current and the reduction in switching speed that is associated with the additional parasitic capacitance.

The best efficiency points of each device are summarized in Table 9-1.

Device	Type	Peak efficiency	Load
SJEP120R125	1200V SiC JFET	96.23%	970W
IPW60R099	600V Si MOSFET	96.42%	973W
IPW90R120	900V Si MOSFET	96.12%	964W
SJEP120R063	1200V SiC JFET x2	95.76%	1057W

Table 9-1: Summary of best efficiency points for different devices in pre-production APR48-ES.

9.3.3 New devices

During the course of the research improved SiC JFETs were developed, with lower channel resistances. Specifically, the SemiSouth SJEP120R100 has a rated on-resistance of 100mΩ, 20% lower than that of the SJEP120R125. The dynamic characteristics of the SJEP120R100 are very similar to those of the SJEP120R125, suggesting that an overall advantage has been obtained through the refinement of SiC JFET technology. Specifically, parasitic capacitances are very similar, as are switching speeds and thermal impedances.

The SJEP120R100 was tested in a telecommunications rectifier to find out whether it could offer a significant performance improvement over the SJEP120R125. The same physical pre-production APR48-ES unit was unavailable, so the SJEP120R100 was tested in a

production APR48-ES rectifier. The production APR48-ES normally utilizes a pair of Fairchild FCH35N60 MOSFETs in its boost converter. The PFC gate drive circuit is the same as that in Figure 9-2, except that R3 and R4 are changed to 22Ω. The same modifications were made to the gate drive circuit as those in Figure 9-3 to allow the Si MOSFETs to be replaced with SiC JFETs. 80Ω, 90Ω, 100Ω and 110Ω resistors were tested for R1 and R2 and 90Ω was found to achieve the highest efficiency. The performance of the SJEP120R100 in the production telecommunications rectifier with 90Ω resistors for R1 and R2 is shown in Figure 9-5 alongside the production rectifier's stock 600V Si MOSFETs (Fairchild FCH35N60) for comparison.

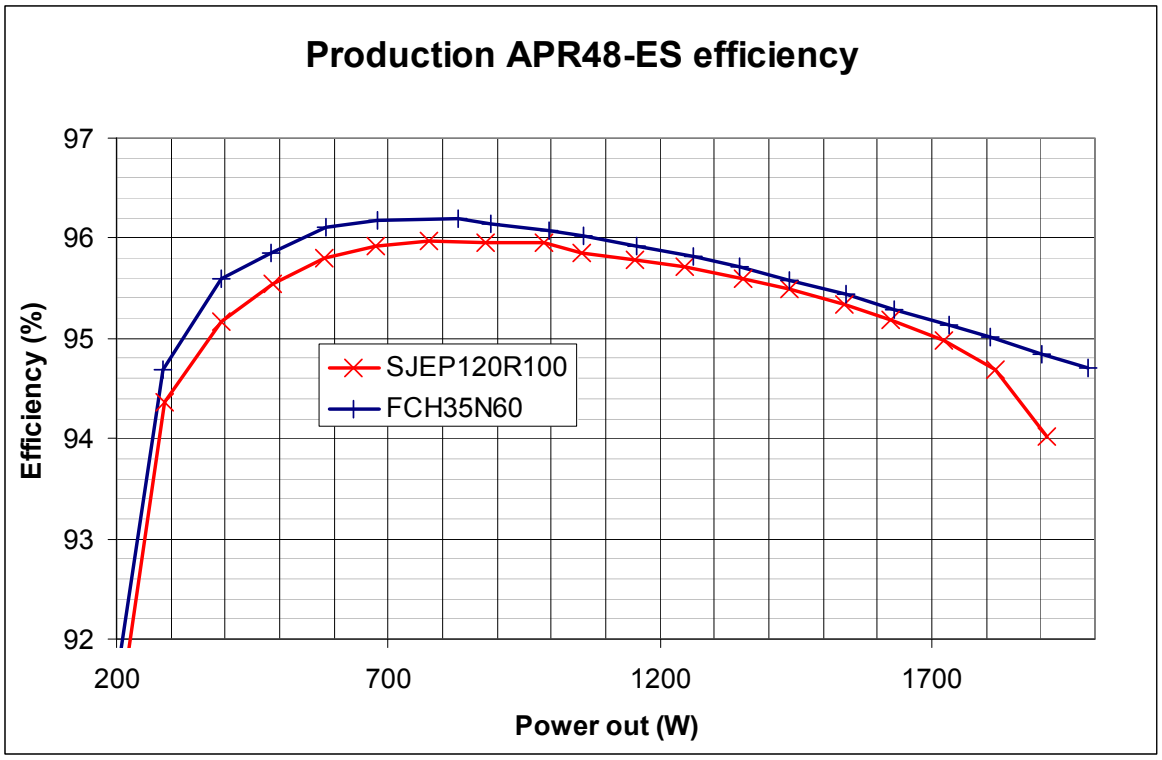


Figure 9-5: Electrical efficiency of the production APR48-ES telecommunications power converter with different transistors in the active power factor correcting boost circuit.

The efficiency of the production APR48-ES is slightly higher with its stock silicon MOSFETs than the new SiC JFETs. The difference is smaller than that observed between the SJEP120R125 and the IPW60R099 in the pre-production rectifier. The highest efficiency achieved by the FCH35N60 MOSFETs was 96.20% at 829W and the highest achieved by the SiC JFETs was 95.97% at 775W. The efficiency of the SiC JFETs decreases substantially towards maximum load. This suggests that the current rating of the SiC JFETs and/or their bias current is slightly inadequate for this application. A reduced

gate impedance would increase the gate bias and may improve efficiency at maximum load with the trade-off being reduced efficiency at lighter load.

The absolute difference in losses between the MOSFETs and JFETs at approximately 800W load is between 1.5-2W. Redesigning the rectifier PCB to accommodate a more sophisticated JFET gate drive circuit could lead to a reduction in losses of 1W or more. The highest efficiency data points for each of the transistors tested in the production telecommunications rectifier are shown in Table 9-2.

Device	Type	Peak efficiency	Load
SJEP120R100	1200V SiC JFET	95.96%	985W
FCH35N60	600V Si MOSFET	96.20%	829W

Table 9-2: Best efficiency data points collected for the production telecommunication rectifier

If SJEP120R125 SiC JFETs had been available at the time that the SJEP120R100 SiC JFETs were tested, or the original pre-production APR48-ES rectifier had been available as a test platform, direct comparisons could have been made between the SJEP120R100 and the SJEP120R125. A comparison of the manufacturer supplied data for each device shows that the SJEP120R100 has slightly higher capacitances and lower drain resistances than the SJEP120R125, but both devices have identical times and energies quoted in the "switching characteristics" sections of their datasheets. It is expected that the switching losses could be slightly higher for the SJEP120R100 than the SJEP120R125, while the conduction losses could be much lower in the SJEP120R100 than the SJEP120R125 due to the SJEP120R100's 20% lower channel resistance.

Direct comparisons cannot be made between the data in Figure 9-4 and Figure 9-5 due to the identified significant differences between the preproduction and production telecommunications rectifiers.

9.3.4 Drive losses

In the APR48-ES, when a SiC JFET was turned on, a sustained gate-source current of approximately 75mA was maintained. To estimate the drive losses that this current represents, the average duty cycle of each JFET was calculated.

The control circuit maintains a boost converter output of approximately 420V while the input to the boost converter is a rectified sine wave. The average of a rectified sine wave is

$$V_{AV} = \frac{2 \cdot V_{pk}}{\pi}. \qquad \textit{Eq 9-32}$$

From *Eq 9-32*, the average voltage for a rectified 230V RMS sinusoid is 207.1V. This translates to an average duty cycle of 50.7%. With PWM applied to one transistor while the other is held on, the drive power dissipated in the pair of JFETs is

$$\begin{aligned} P_{drive} &= V_{gs} \cdot I_g \cdot (1 + D) \\ &= 3 \cdot 0.075 \cdot 1.507. \\ &= 0.34W \end{aligned} \qquad \textit{Eq 9-33}$$

The gate drive circuit operates from a floating regulated 13V supply. The power drawn from this supply to drive the JFETs in steady state is approximately 1.47W. Redesigning the auxiliary power supply transformer to deliver a lower output voltage could allow this figure to be reduced, closing the gap between the silicon and SiC transistor performance.

9.3.5 Thermal considerations

The IPW6R099 silicon MOSFET used in the pre-production telecommunications power converter and SJEP120R125 SiC JFET are both packaged in similar TO-247 cases. Despite having the same case, the SJEP120R125 has a much higher junction to case thermal impedance than the IPW6R099, suggesting that it may have a much smaller die. The cases of a SJEP120R125 SiC JFET, IPW6R099 MOSFET and ST55MN60N MOSFET were opened. Figure 9-6 illustrates the dramatic difference in die size that was observed.

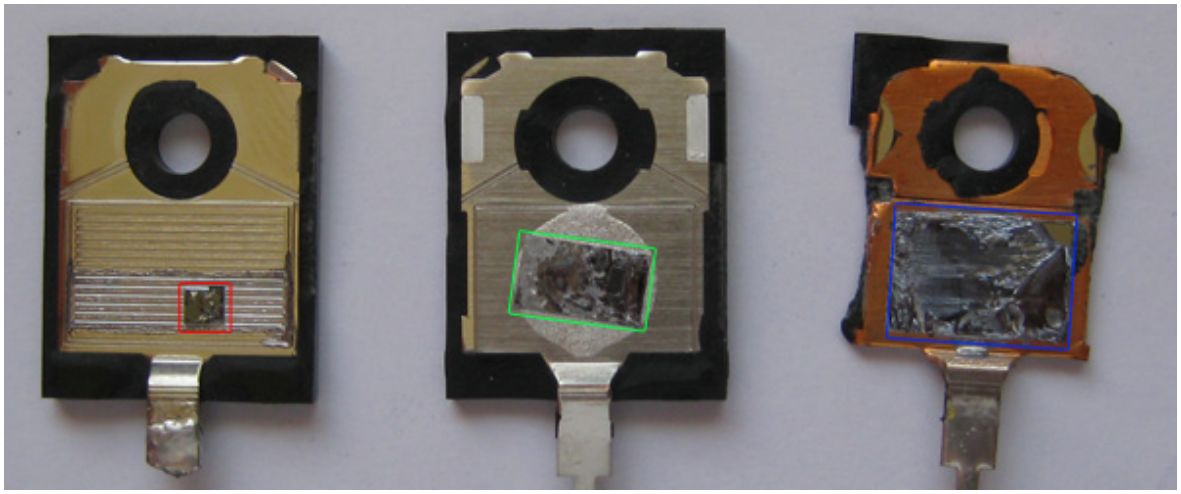


Figure 9-6: The SJEP120R125 SiC JFET die (red, left) is much smaller than those of IPW6R099 (green, centre) and ST55MN60 (blue, right) silicon MOSFETs

The die sizes and thermal resistances of the three transistors are summarized in Table 9-3.

Device	Die area	Junction-case thermal impedance
SJEP120R125 SiC JFET	$4mm^2$	1.1°C/W [Appendix C]
IPW6R099 Si MOSFET	$28mm^2$	0.5°C/W [128]
ST55MN06 Si MOSFET	$70mm^2$	0.36°C/W [129]

Table 9-3: Die sizes and thermal impedances of three transistors

If the SJEP120R125's gate-source current is held constant at 100mA and its gate-source voltage allowed to vary, the $R_{DS(on)}$ closely matches that of the IPW60R099CP over a wide temperature range as shown in Figure 9-7. Larger losses result in a higher operating temperature which in turn leads to greater losses. This thermal 'multiplier' effect amplifies any difference in loss between the two transistors.

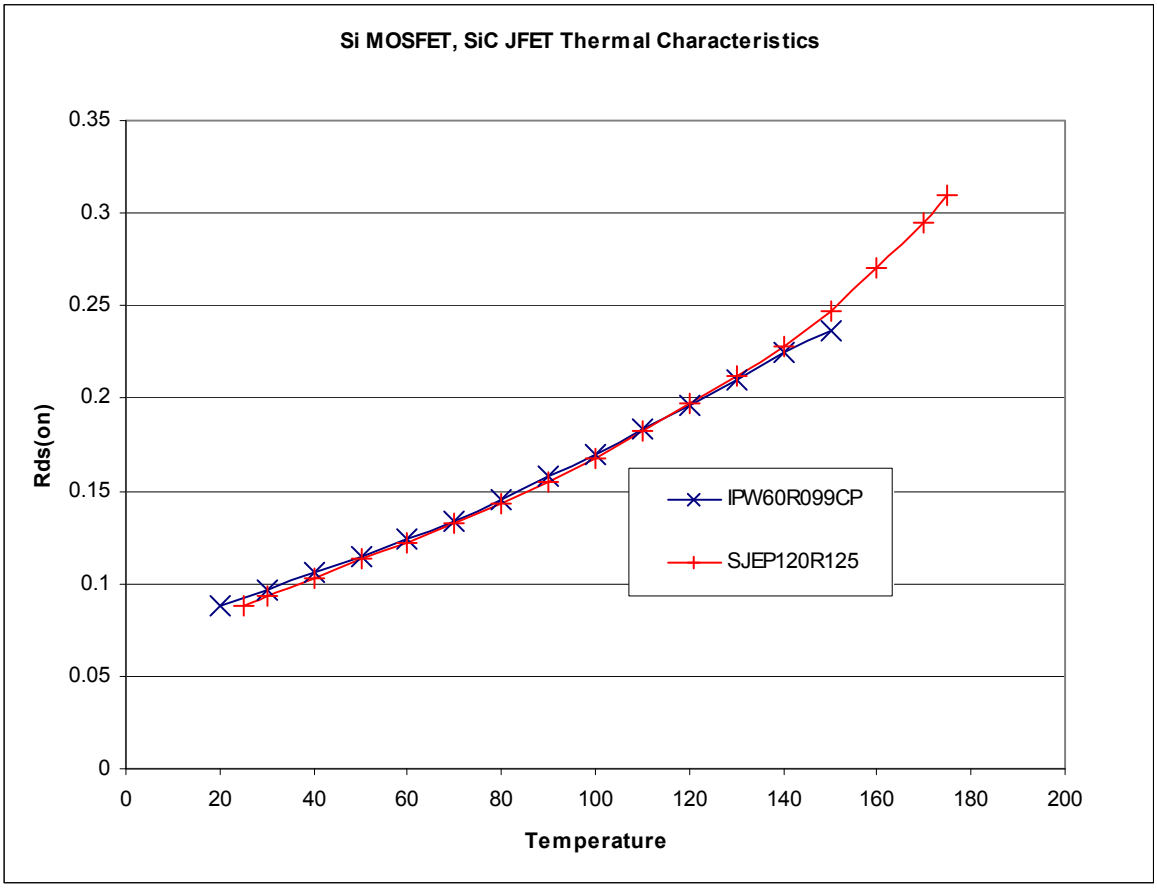


Figure 9-7: Channel resistance of the Si MOSFET and SiC JFET against temperature

Because the SJEP120R125 has a junction to case thermal resistance of 1.1°C/W [Appendix C] while the IPW60R099CP has one of 0.5°C/W [128], the SJEP120R125 will operate at a higher temperature than the IPW60R099CP, consequently exhibiting larger conduction losses. Differences in thermal performance will become more significant at higher power levels, because larger transistor currents will lead to increased overall dissipation.

9.4 Impact of findings

1200V normally-off SiC JFETs were shown to perform close to the level of the best 600V silicon MOSFETs available at the same time. Simple modifications to typical MOSFET drive circuits to accommodate SiC JFETs do not result in overall higher efficiency, though it may be attainable through the use of more sophisticated JFET driver circuits. The significant cost difference between the SiC JFET and the silicon MOSFET does not warrant the use of present day SiC JFETs in single phase telecommunications rectifiers.

The performance of SiC JFETs compared to 900V silicon MOSFETs suggests that they could be of substantial benefit in applications which require blocking voltages in excess of 600V. In particular, the performance of SiC JFETs should be evaluated in applications that typically utilize 900V silicon MOSFETs.

The differences in thermal impedance between the SiC JFETs and silicon MOSFETs highlight the importance of thermal design in any circuit where SiC JFETs are to be used.

The particularly poor results achieved by the SJEP120R063 suggest that paralleling the normally-off JFETs, for improved $R_{DS(on)}$, may not result in better overall performance in applications where the current is small enough to be carried by a single JFET. If gate ringing was a significant factor in the performance of the SJEP120R063, a TO-247 case with more than three terminals could offer an improvement by separating the gates and/or sources of the co-packaged devices.

Because SJEP120R125 JFETs were not available at the time that SJEP120R100 JFETs were tested, it was not possible to draw direct comparisons in the same test circuit. A comparison of the manufacturer datasheets suggests that the SJEP120R100 has parasitic capacitances that are 10-20% higher than the SJEP120R125 and 11% lower typical channel resistance at 25°C. Interestingly, the SJEP120R100 and SJEP120R125 have the same rated channel resistances at 125°C. The increased capacitance of the SJEP120R100 is expected to contribute to slightly higher switching losses while its lower channel resistance at low temperatures should improve conduction losses. The overall performance of the SJEP120R100 and SJEP120R125 are expected to be very similar in most applications.

Chapter 10 Three-phase cyclo-converter application

600V is typically an adequate rating for transistors in single phase power supplies as it is larger than the peak phase to neutral voltage during a high-mains condition in a 230V utility system. Transistors in three-phase power supplies often have to withstand line to line voltages, which are larger by a factor of √3. At high mains, 600V MOSFETs are unsuitable in 400V and 415V three-phase systems. Typically, power converters operating from such systems utilize 900V MOSFETs. 480V three phase systems may demand blocking voltages as high as 1000V. The SJEP120R125 and SJEP120R100's 1200V ratings make them eminently good candidates for many three phase applications and are expected to exhibit higher switching speeds than 900V silicon MOSFETs.

A 400/415V three-phase cyclo-converter that uses 900V silicon MOSFETs was in development at Eaton. A lower voltage version of this cyclo-converter, for 208V systems, had already been developed to a working prototype stage at the time of this research, while the 400/415V version was in early development stages. To evaluate SiC JFETs as potential candidates for the future 400/415V converter, they were tested in the 208V prototype converter.

10.1 Cyclo-converter theory

The three-phase cyclo-converter application utilises a topology consisting of three pairs of back-to-back transistors between the three mains phases and a common bus. Each back-to-back pair of transistors forms a quad-state switch, capable of behaving like an open circuit, closed circuit or a diode of either polarity. A neutral point is created by a capacitive divider. The output is connected between this neutral point and the common bus, forming a single-stage three-phase to single-phase AC to AC converter.

Building a resonant tank around the load allows power conversion to be controlled via switching frequency. The addition of a transformer and rectification circuit to the resonant tank forms a complete three-phase AC to low voltage DC power converter as shown in Figure 10-1.

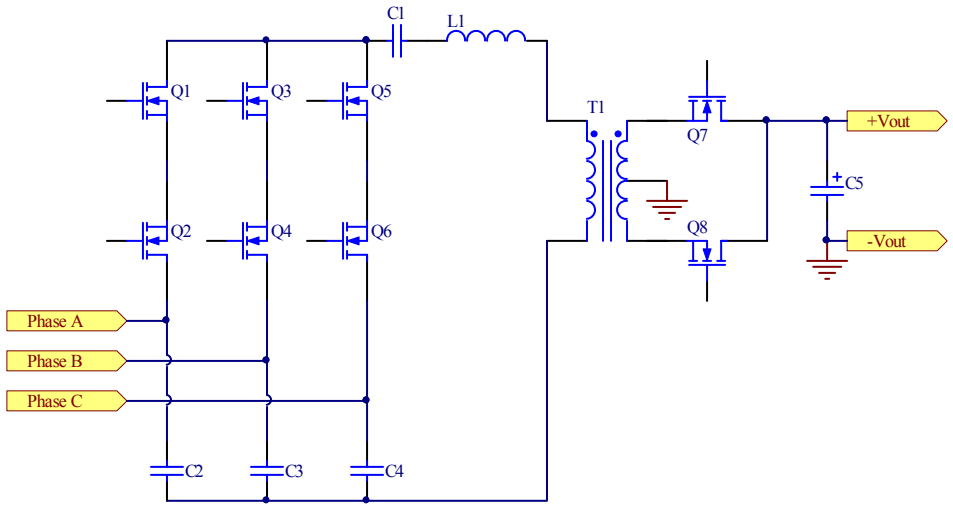


Figure 10-1: Three phase cyclo-converter topology

Like the power factor correction circuits in the latest single-phase telecommunications rectifiers, the cyclo-converter has only two series conducting semiconductors at any time. However the cyclo-converter does not require additional primary-side transistors like those typically found in the bridge of a DC-DC stage in a single phase telecommunications rectifier. This means that current only has to flow through two series semiconductors instead of four on the primary side of the transformer, resulting in significantly lower conduction losses than most single phase converters. The cyclo-converter uses synchronous rectification on its secondary side, similar to many modern single phase telecommunications rectifiers.

A variety of specialized switching patterns are used during different parts of the mains cycle. Using the naming convention outlined in section 2.3, unity power factor is achieved by varying the on-time ratio of the small and medium phases.

10.2 Gate drive modifications

In the three phase cyclo-converter prototype, each phase is connected to a common output node via a bidirectional switch. Each switch consists of a pair of Infineon IPW6R045 MOSFETs and is driven by its own gate drive circuit. A single gate drive circuit for one such pair of MOSFETs is shown in Figure 10-2. Resistors R1 and R2 limit peak gate currents and dampen ringing. Ferrite beads L1 and L2 provide suppression to high frequency ringing above 50MHz. The drive circuit is powered from an auxiliary flyback converter.

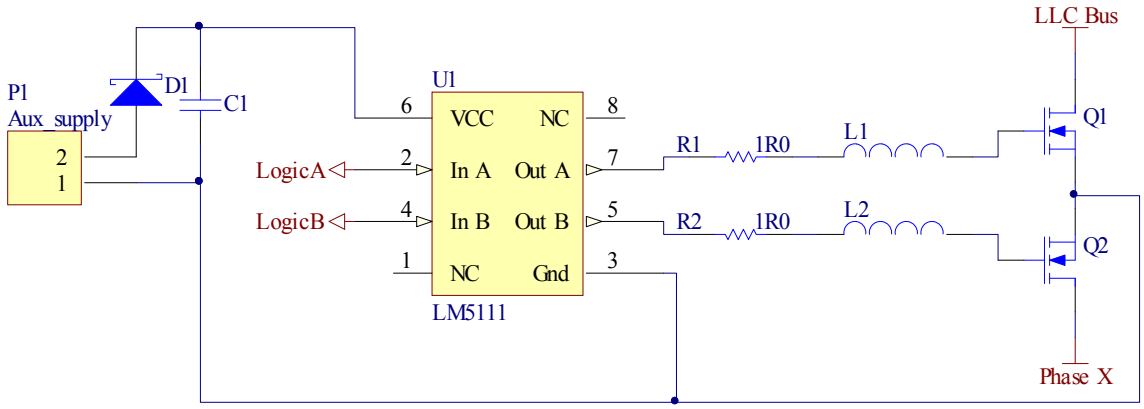


Figure 10-2: Original gate drive circuit from one leg of the three phase cyclo-converter.

The gate drive circuit was originally constructed from surface mount components as shown in Figure 10-3, to allow critical loop areas to be kept very small. The gate drive circuit is mounted on the opposite side of the PCB to the MOSFETs to further minimize parasitic inductances and the MOSFETs are mounted deep in the circuit board, to minimize their source lead inductance.

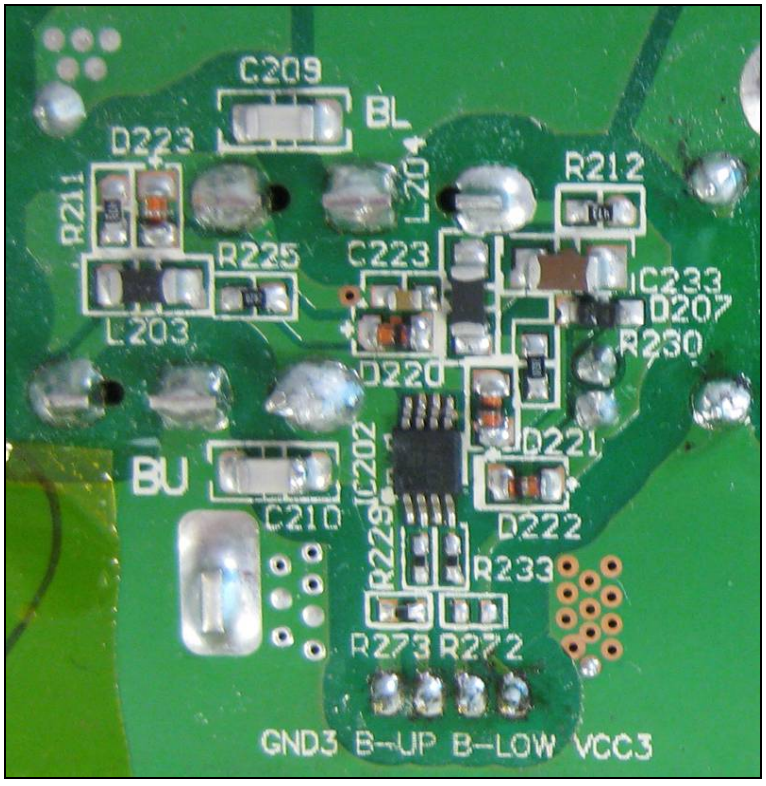


Figure 10-3: Cyclo-converter gate drive circuit

To accommodate SiC JFETs, several modifications were made to the gate drive circuit as shown in Figure 10-4. Resistors R2 and R4 limit the continuous gate current, while the paralleled capacitors C1 and C2 provide low impedance AC paths to ensure rapid turn-on and turn-off. R1 and R2 limit the current magnitude through the capacitors to minimize ringing. C2 and C3 also have the advantageous effect of creating a charge-pump effect, resulting in a small negative voltage being applied to the gate of either JFET during turn-off. This improves turn-off transition speed and provides some immunity to false turn-on.

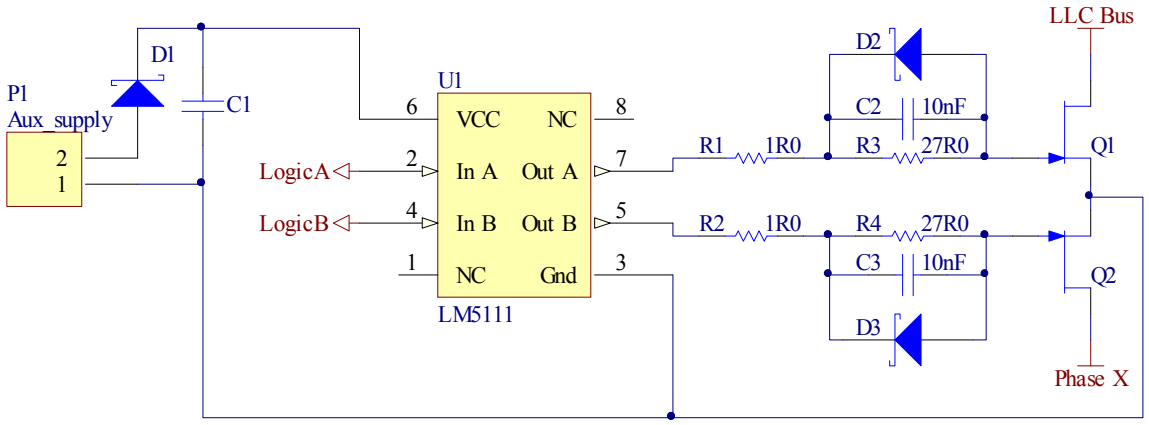


Figure 10-4: Cyclo-converter gate drive modified to accommodate SiC JFETs.

Although D2 and D3 limit the extent of the charge-pumping effect, tests confirmed that they significantly reduce gate voltage ringing. It was further observed that the cyclo-converter topology is particularly sensitive to parasitic gate-drain capacitance.

Despite the presence of D2 and D3 as well as the negative gate-source voltage generated by C2 and C3, erroneous turn-on of Q1 and Q2 was observed. In this application erroneous turn-on of the SiC JFETs resulted in a phase-phase short circuit condition, with the associated fault current causing destruction of the JFETs.

To increase the immunity of the circuit to gate-drain capacitive effects, the sources of the JFETs were raised above the floating ground. This allowed U1 to apply a small negative bias to the gates during off times. The source voltage was lifted by the addition of a diode, D4 as shown in Figure 10-5 with associated biasing and decoupling.

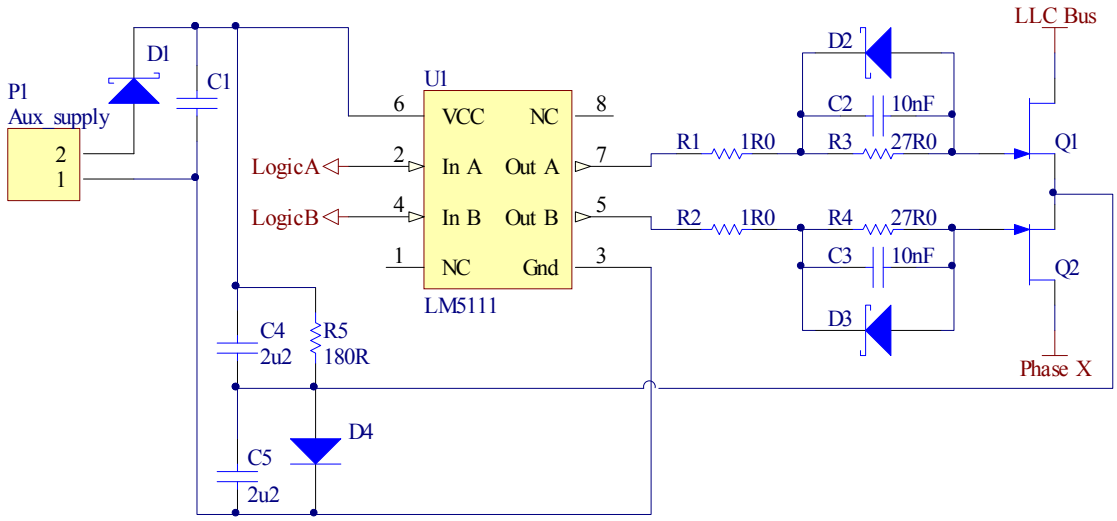


Figure 10-5: The source terminals of JFETs Q1 & Q2 are lifted above the floated ground by diode D4's forward voltage drop

The effect of the small negative gate-source voltage generated across D4 can be observed in Figure 10-6, with some charge-pumping action from C2 and C3 also visible near the turn-off transitions.

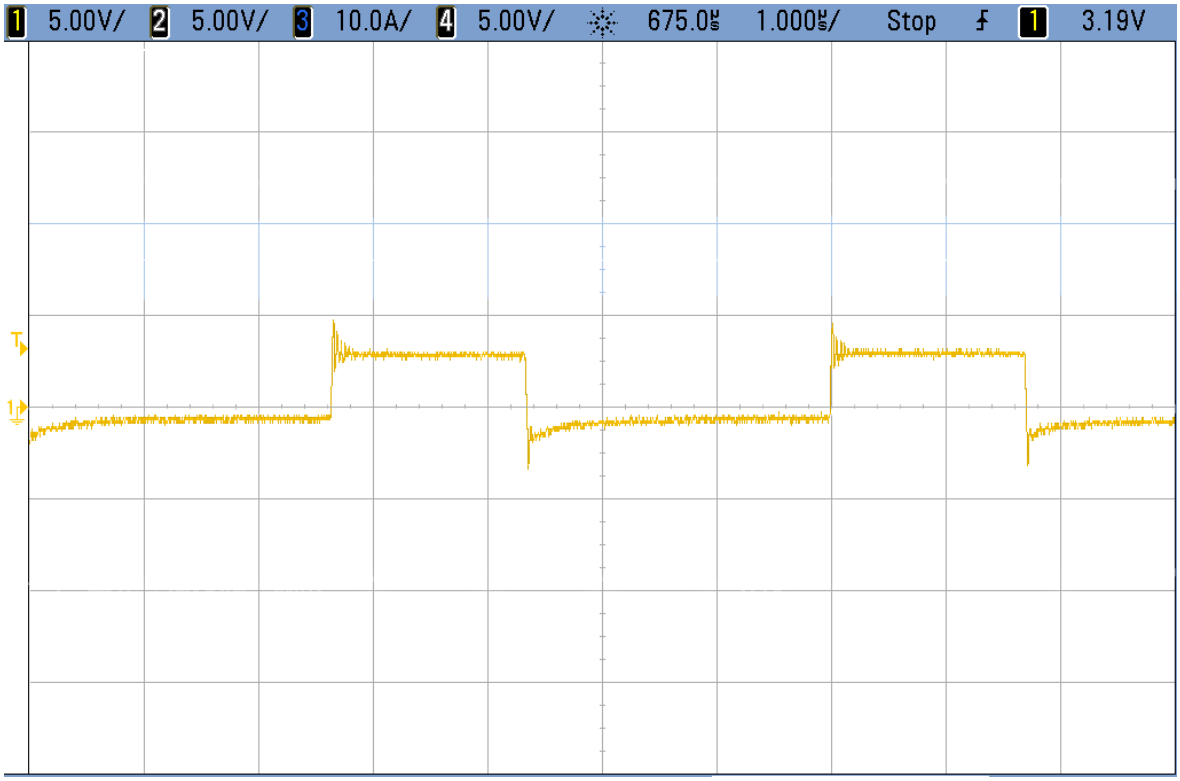


Figure 10-6: Gate source voltage for Q1 swinging below zero volts due to D4's voltage drop.

Correct circuit operation was observed for short periods of time (around 2ms) followed by intermittent switching problems that lead to excessive resonant currents and activation of protection circuits. Physical positioning of differential oscilloscope probes for circuit measurements was found to significantly affect switching performance, indicating significant susceptibility to parasitic capacitances. To provide further immunity to parasitic circuit characteristics, the voltage drop created by D4 in Figure 10-5 was instead replaced by a floating DC power source (BT1) connected in series with the existing supply (P1) as shown in Figure 10-7. The source terminals of the pair of JFETs were connected to the centre point of BT1 and P1, allowing U1 to pull the JFET gates to -3V, during turn-off, whilst still pulling up, during turn-on, to the same potential as before.

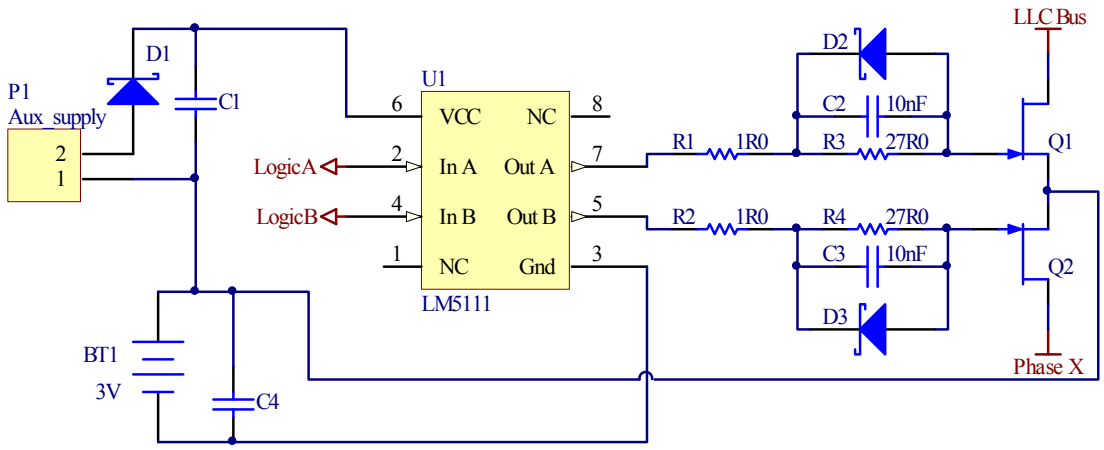


Figure 10-7: Single leg of finalized gate drive circuit for three phase cyclo-converter.

To minimize parasitic elements the modifications were implemented using surface mount components, with the exception of R3 and R4 which were necessarily constructed from pairs of small through-hole resistors to meet power dissipation requirements.

Figure 10-8 shows the gate-source voltages of a pair of JFETs in the cyclo-converter. When turned on, the gate-source voltage drop is approximately 3V at the chosen gate current and at turn-off is held at -3V. The logic signals are also shown, with no significant delays visible between the command signals and the gate voltages.

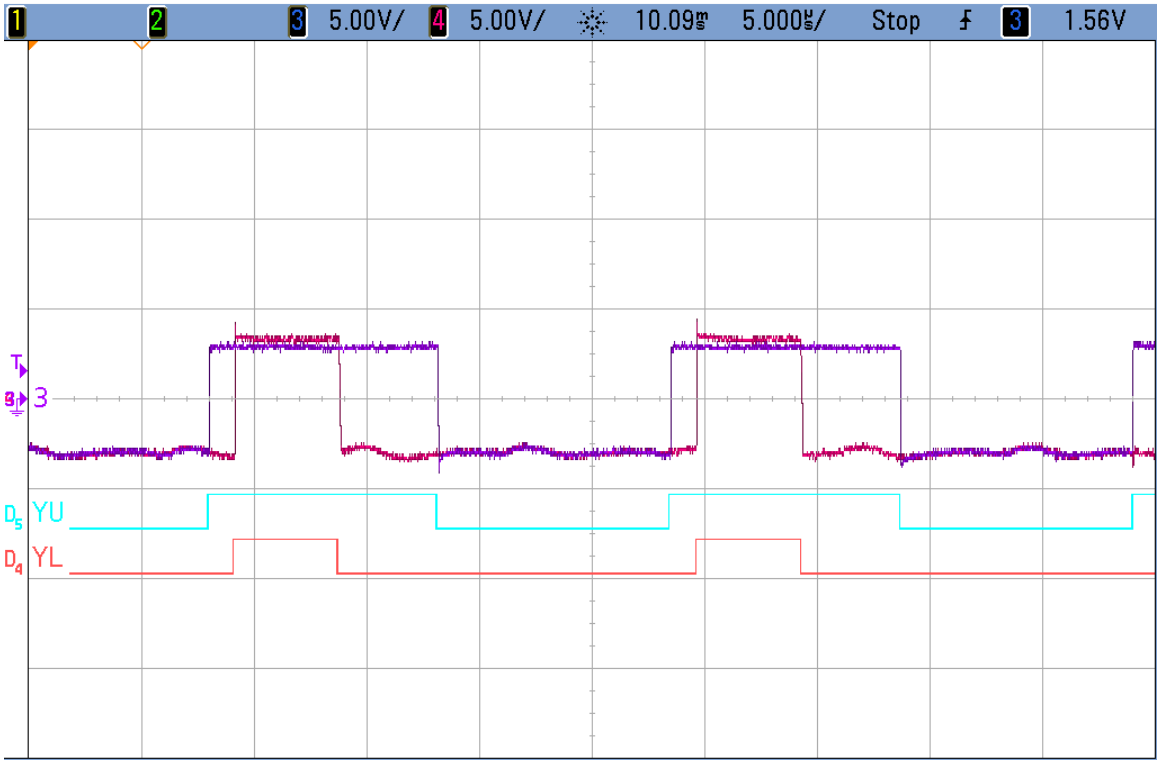


Figure 10-8: Lower JFET (purple trace 3) and upper JFET (pink trace 4) gate-source voltages. The logic command signals for the lower and upper JFETs are shown on channels D4 and D5 respectively.

The significant negative gate voltage applied by the revised gate drive circuit in Figure 10-7 solved the erroneous switching problems that were observed previously.

10.3 All SiC cyclo-converter

After observing acceptable switching characteristics in the SiC JFET leg of the three-phase cyclo-converter with the gate drive circuit in Figure 10-7, the gate drives of the other two phases were also modified and their MOSFETs replaced with SiC JFETs. The same construction techniques were adhered to as for the first phase.

Testing of the cyclo-converter with exclusively SiC JFETs in all three legs revealed further switching problems and excessive resonant current. Figure 10-9 shows the gate-source voltage across the lower JFET in phase A as well as the drain-drain voltage across both SiC JFETs in phase A. The gate-source voltage can be seen to sag, resulting in the (negative) drain-drain voltage increasing in magnitude erroneously towards the lower right of Figure 10-9. The gate-driver circuit's power source is shown in purple in Figure 10-9 and did not exhibit significant sagging, suggesting that the floating power supply was adequate.

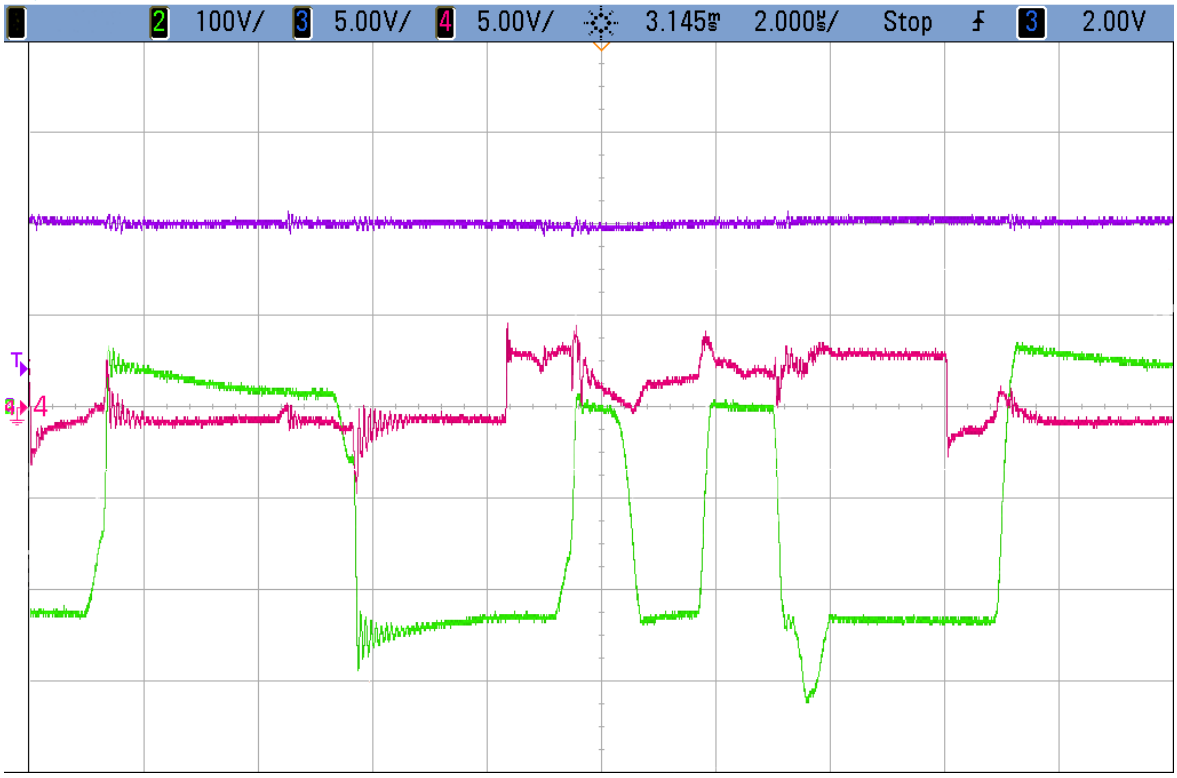


Figure 10-9: Lower JFET gate drive (4, Pink), drain-drain voltage across pair of JFETs (2, Green) and gate drive supply (3, purple).

The sustained gate current during turn-on was increased from approximately 150mA to 300mA by reducing the values of R3 and R4 from 27Ω to 13.5Ω. This significantly higher bias point resulted in a decrease in the amount of sag on the JFET gate voltage and the false turn-off behaviour stopped.

Despite driving the SiC JFETs with close to 300mA of sustained bias current, excessive resonant tank currents were still observed, as shown in Figure 10-10. Peaks in excess of 40A were observed and caused corresponding increases in voltage drop across the JFET channels. This resulted from the 40A peak current vastly exceeding the 15A ratings of the SiC JFETs.

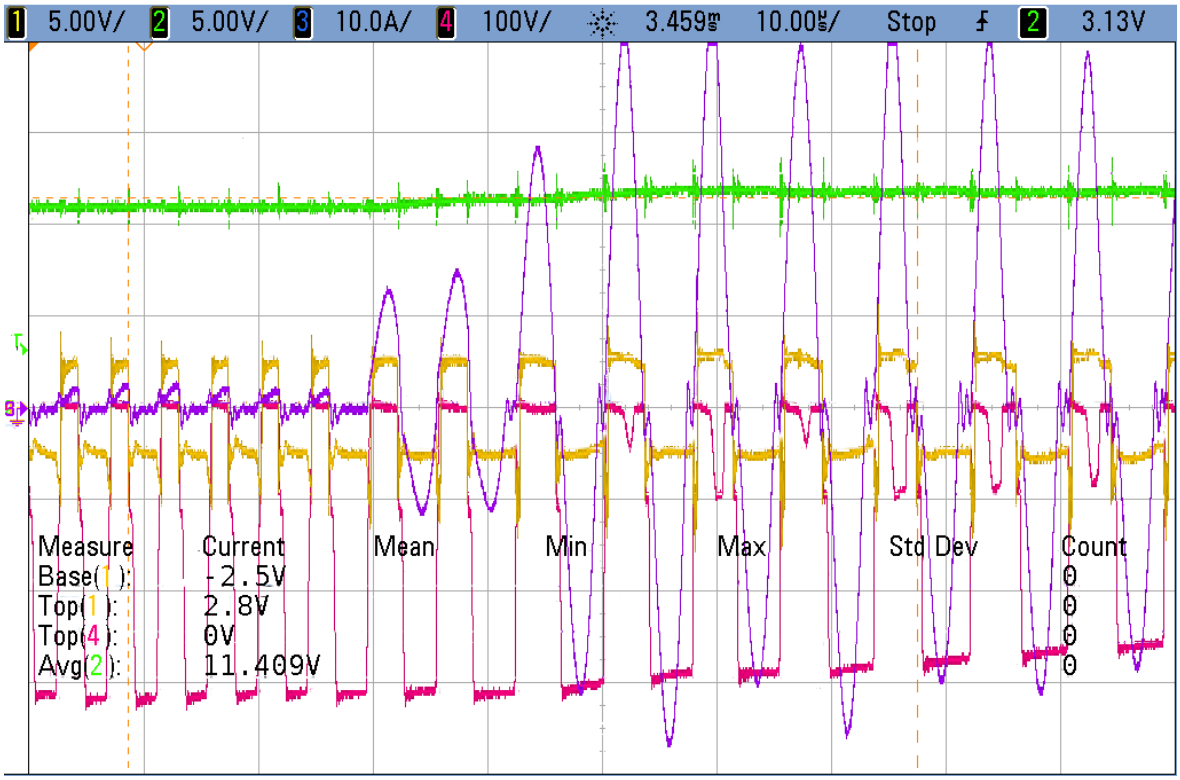


Figure 10-10: Excessive resonant tank current (3, purple) causing the voltage drop across a JFET's channel (4, pink) to rise as the JFET's current rating is exceeded. Also shown are the JFET's gate-source voltage (1, yellow) and the converter's output voltage (2, green).

The cause of the excessive resonant tank current was found to be that the control circuitry in the prototype was rapidly decreasing the switching frequency (and therefore increasing converter power) to bring the output voltage up to the correct set point. The incorrectly tuned control circuit can be seen bringing the output voltage (green) in Figure 10-10, from 10.5V to 12.5V in approximately 20µs. The failure of the SiC JFETs to conduct 40A resulted in the converter repeatedly shutting down before attempting to start up again, resulting in oscillation.

With silicon MOSFETs, oscillation is less of an issue because 40A does not exceed the maximum ratings of the IPW90R045 MOSFETs and thus did not cause spurious rises in drain-drain voltage in the original prototype circuit.

The 400/415V cyclo-converter operates at significantly lower currents than the 208V version to achieve the same power rating. If SiC JFETs are adopted into the 400/415V version and start-up currents are found to be excessive, these can be limited via software

changes in the cyclo-converter's control circuitry. For practical testing purposes, the issue can simply be avoided in the existing 208V prototype by pre-charging the output capacitors to approximately 11V before starting the converter. Figure 10-11 shows excessive resonant tank current (purple) causing spurious converter oscillation (left), while pre-charging the capacitors results in significantly reduced starting current and no oscillation (right).

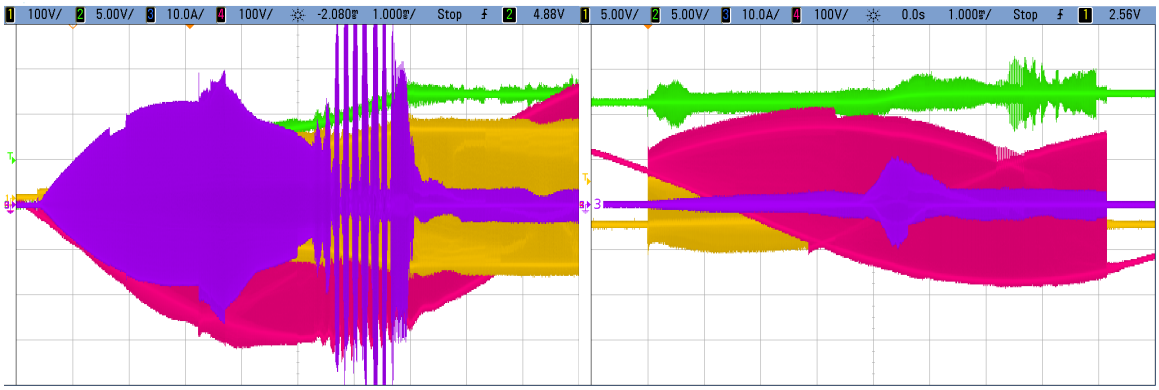


Figure 10-11: Excessive resonant tank current (10A/div) causes spurious oscillation (purple, left), while pre-charging the output capacitors reduces the current to a suitable level (purple, right). Also shown are the resonant tank voltage (1, yellow), the voltage across a pair of JFETs (4, pink) and the converter's output voltage (2, green).

10.3.1 Switching performance

The cyclo-converter incorporates a proprietary switching scheme that includes three distinct switching patterns for different parts of the three-phase input waveform. During the main switching pattern, each phase is connected to the common bus once per period of the output voltage.

When the magnitudes of two of the phases are very similar, a different switching pattern is used. This switching pattern results in the medium and small phases only turning off once for every second output period. Therefore, a factor of 0.5 must be used when calculating switching loss power from per transition energy.

Around zero crossings, a third switching pattern is used. Here, the small phase has almost no voltage and should carry almost no current to maintain a high power factor. The small phase is simply left off in this mode resulting in no switching losses.

Figure 10-12 shows a three-phase mains voltage waveform with regions around the zero and magnitude crossing regions highlighted (in orange and green respectively). The un-highlighted regions of the waveform employ the standard switching pattern.

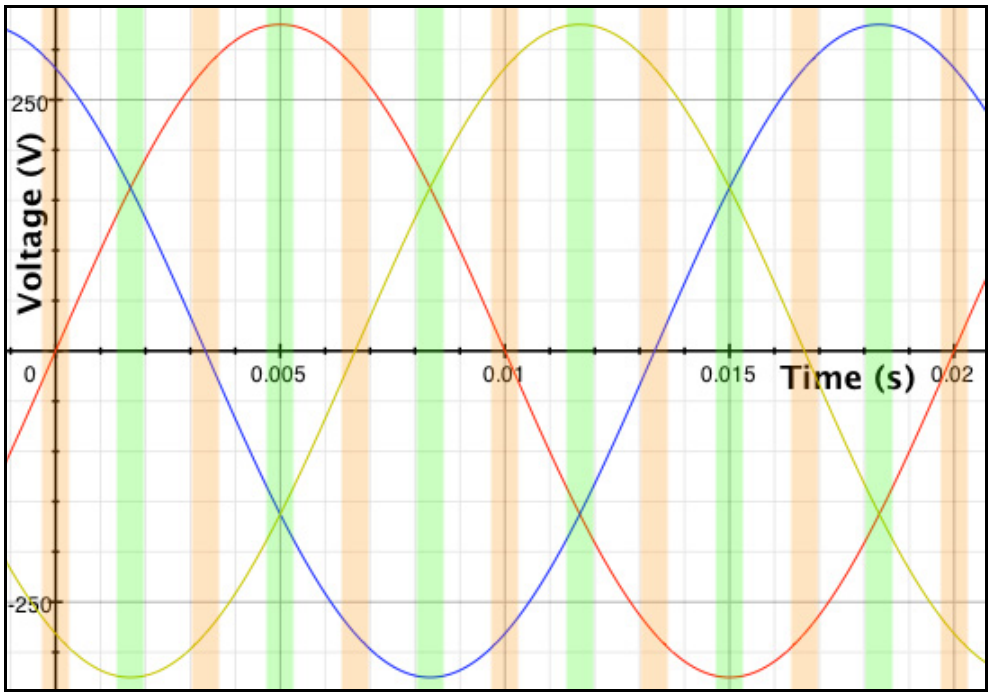


Figure 10-12: Three-phase waveform showing regions around zero crossings (orange) and magnitude crossings (green)

The voltage across and current through each pair of JFETs was observed during each of the three switching modes at a very light load of 50W. By integrating the product of the voltage and current with an oscilloscope, the turn-off energy was calculated for each combination and is summarized in Table 10-1 (measurement accuracy of ±3%). The values marked * indicate the magnitude crossing condition where the small and medium phases only dissipate the calculated turn-off energy every second output period. The proportion of the mains cycle spent in each of the proprietary switching patterns is provided for weighting. Some details of the switching patterns are described in [59].

	Small (µJ)	Medium (µJ)	Large (µJ)	Total per cycle (µJ)	Proportion
Main Switching	10.312	6.191	6.621	26.124	77%
Magnitude Cross	9.18*	25.547*	9.941	27.30	15%
Zero Cross	0	13.652	6.211	19.863	8%

Table 10-1: The turn-off loss energies per turn-off for each phase (small, medium large) during each switching pattern (main, magnitude cross and zero cross).

The output frequency was measured and found to be approximately 150kHz with the light load. The main switching mode is used most of the time with the other modes only occurring briefly around each magnitude or zero crossing. By weighting the switching energies of the different loads based on the time spent in each mode, the overall switching loss power was calculated as 3.6W.

10.3.2 Drive losses

The drive circuitry for each leg floats with the voltage at the midpoint of each pair of JFETs. The potential of the drive circuitry relative to ground changes with the switching of the transistors at very high slew rates. This makes the drive circuits very sensitive to capacitive coupling to ground. As a result, it is almost impossible to measure drive losses directly without significantly altering switching performance.

A flyback converter provides power to each JFET driver circuit via different windings on its flyback transformer. With the mains input to the JFETs removed, the JFET driver circuits were disabled one at a time and the changes in power flowing into the flyback converter were measured. This provides an estimate of the ballpark drive losses, but cannot account for increased drive losses due to Miller effects because of the removal of the mains connection.

Power drawn by the flyback converter was measured using a high precision Yokogawa WT230 three phase power meter. The measurements for each phase are shown in Table 10-2. Each delta measurement in Table 10-2 had an accuracy of ±40mW.

JFET Pair	Drive power consumed
Red	2.5W
Yellow	2.7W
Blue	2.2W

Table 10-2: Drive losses for each pair of JFETs

In addition to the drive losses in Table 10-2, each JFET driver receives a small amount of power from a floating -3V supply. The current drawn from each supply was measured

(with the mains disconnected) and found to be approximately 40mA, representing an additional 0.12W (±14mW) of drive losses, resulting in a total drive loss figure of 7.5W.

Because the JFETs are driven from an 8V floating supply, yet their gate-source voltage drop is approximately 3V, 63% of the drive power is dissipated by the gate resistors and gate driver circuitry. It is possible that the gate drive power could be reduced by more than 50% by redesigning the auxiliary power supply circuitry to deliver a lower drive voltage.

An additional standing loss of 2.9W is also drawn from the flyback converter to generate the 5V, 3.3V and 1.8V supplies to the DSP and FPGA circuitry. Primary side losses in the cyclo-converter, excluding conduction losses, are summarized in Table 10-3 alongside the measurement accuracies. The total drive loss is 14.0W ±0.2W.

Item	Power (W)	Accuracy (W)
Switching losses	3.6	0.04
Gate drive losses	7.5	0.13
Logic circuit consumption	2.9	0.04
Total	**14.0**	**0.21**

Table 10-3: Summary of primary side losses excluding conduction.

10.4 Back-to-back blocking behaviour

The voltage waveforms observed between the drains of each pair of SiC JFETs in the cyclo-converter differed significantly to those observed with silicon MOSFETs. Closer investigation revealed that a phenomenon was occurring where both JFETs in a pair were blocking substantial voltages simultaneously. The phenomenon occurs because of parasitic capacitance effects when the common node between a pair of JFETs' source terminals is more negative than either JFET's drain terminal. The voltages blocked by each JFET in a pair partially cancel each other out, resulting in a drain-drain voltage across the bidirectional switch identical to that observed with silicon MOSFETs. Figure 10-13 shows the relative polarities and magnitudes of the voltages in the transistor pairs. On the left, a pair of MOSFETs block a voltage of magnitude Vsw. Q1 blocks the entire voltage while Q2 does not block any voltage and the common node between Q1 and Q2 is at a potential of 0V. On the right, a pair of SiC JFETs also block a voltage of magnitude V_{SW}. However

Q2 is blocking a voltage of magnitude V2, causing Q1 to block the sum of Vsw and V2. The common node between the JFETs is at a potential of –V2.

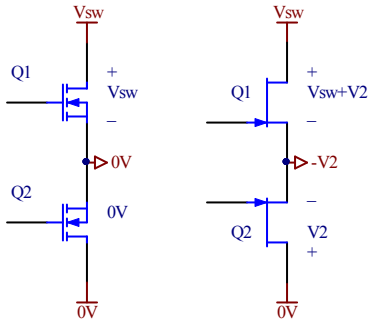


Figure 10-13: MOSFETs blocking a voltage Vsw (left) and JFETs (right) blocking the same voltage with the back-to-back blocking behaviour

10.4.1 Affected area

The back-to-back blocking behaviour with SiC JFETs only occurs during certain portions of the mains cycle. Several of the switching patterns in the prototype cyclo-converter satisfy these requirements and the phenomenon was observed as being most pronounced near mains magnitude crossing points.

The envelope of the back-to-back blocking effect is visible in the drain-source voltages of the JFETs, outlined with yellow in Figure 10-14. When silicon MOSFETs were used, the patterns outlined in yellow were not present. The *MAG_X* logic signal indicates the approximate regions around each magnitude crossing where a different switching pattern is used and the maxima of the envelopes are observed. A green vertical line indicates a region several degrees before a magnitude crossing during the standard switching sequence where the phenomenon is particularly pronounced. This region has been chosen as a focal point for parasitic capacitance analysis.

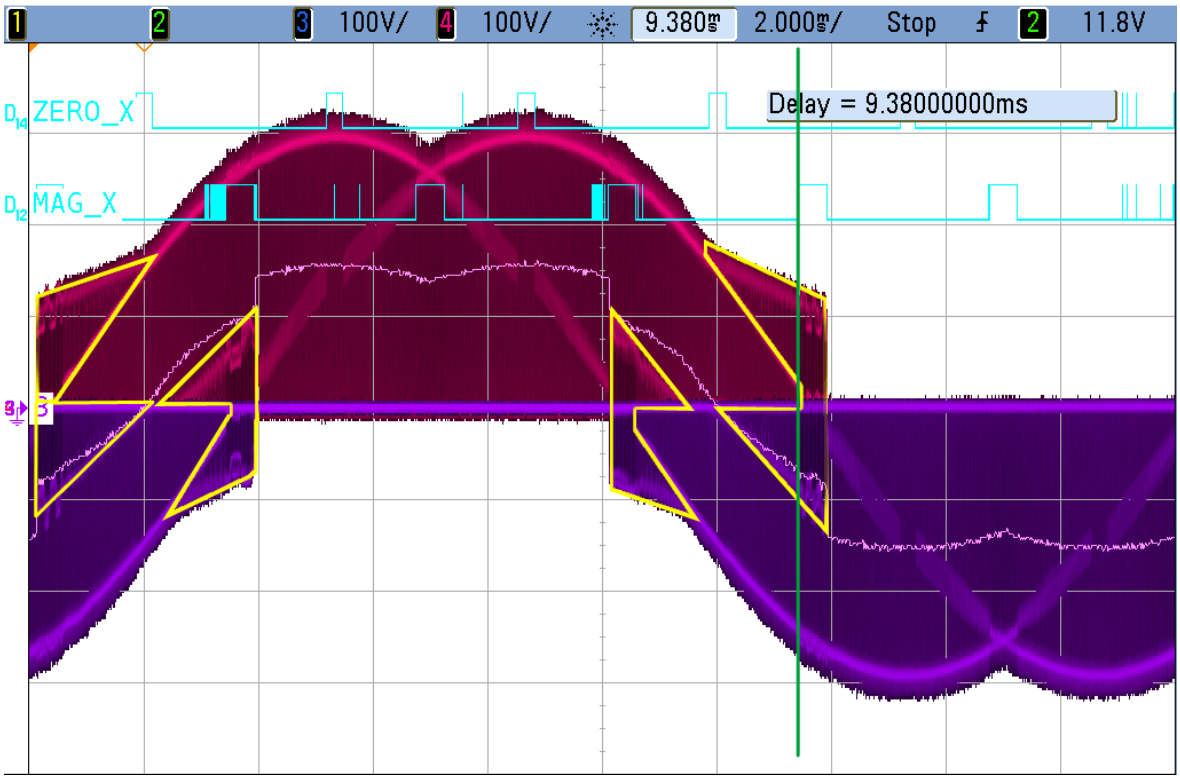


Figure 10-14: Drain-source voltages of the upper (pink) and lower (purple) JFETs with the back-to-back switching phenomenon highlighted in yellow. The region used in the analysis is indicated by a vertical green line.

10.4.2 Output capacitance modelling

The drain-source capacitance of the SJEP120R125 is quoted as 90pF at 100V [Appendix C], and the output capacitance of the MOSFETs originally used in the prototype are quoted as 300pF at 100 volts [130]. It is well known that MOSFET output capacitances increase with decreasing voltages and this is also true of the SiC JFETs, albeit to a lesser extent. The output capacitances of both devices were measured at zero volts with gate-source short circuits. The SJEP120R125 SiC JFET had a capacitance of 1.2nF compared to 53nF for the silicon MOSFET. This large difference has major consequences for the way that charge is shared between the small phase transistors during a large to medium transition of the other two phases. To allow the output capacitance to be used in computer based iterative calculations in sections 10.4.5 and 10.4.6, the voltage dependent output capacitance of the SJEP120R125 was modelled over a broad voltage range by fitting a curve to the manufacturer supplied information. *Eq 10-34* defines the curve that was used for the SJEP120R125, where v is the drain-source voltage in volts and C_{OSS} is the output capacitance in picofarads.

$$C_{OSS} = 620 \cdot e^{-0.33v} + \frac{4000}{v+8} + \frac{190}{80\left(\left|v-5\right|+190\right)} + 3 \qquad \textit{Eq 10-34}$$

The capacitance model in for the SJEP120R125 in *Eq 10-34* achieves a good fit, as shown superimposed over a portion of the manufacturer supplied graph [Appendix C] in Figure 10-15.

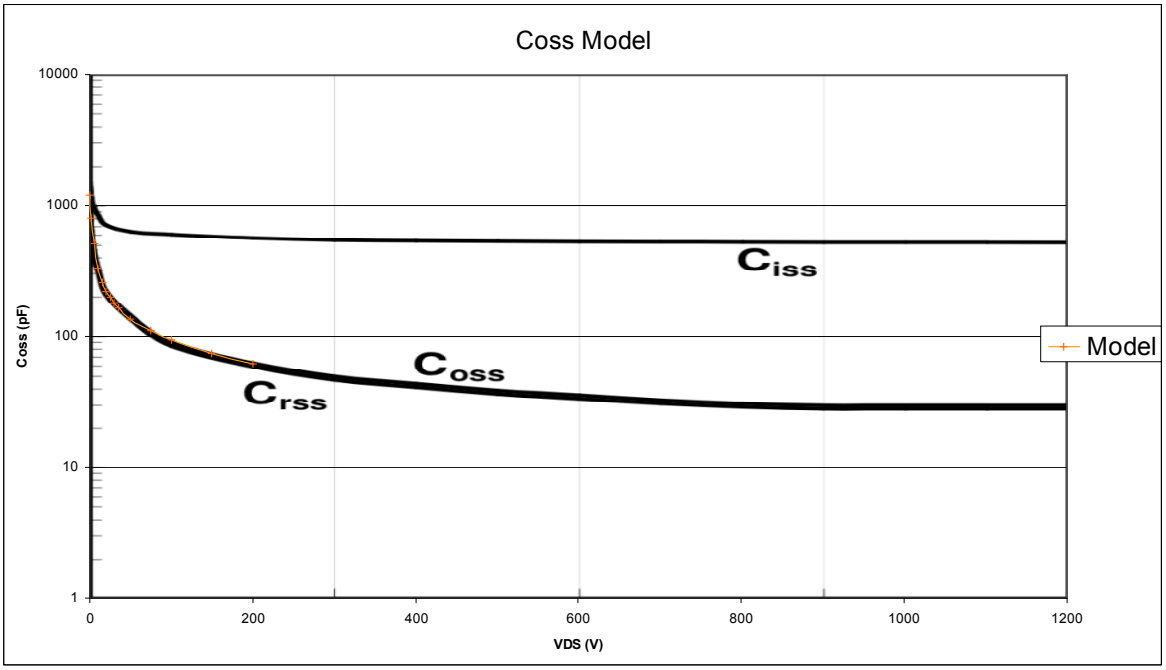


Figure 10-15: The C_{oss} model superimposed over the manufacturer supplied curve

The IPW6R099 silicon MOSFET's voltage-capacitance relationship is more non-linear than the SJEP120R125's, making it impractical to model without piecewise equations. Instead, 20 discrete points were fitted to the manufacturer-supplied curve [130] as shown in Figure 10-16. These were used during the iterative calculations in section 10.4.5.

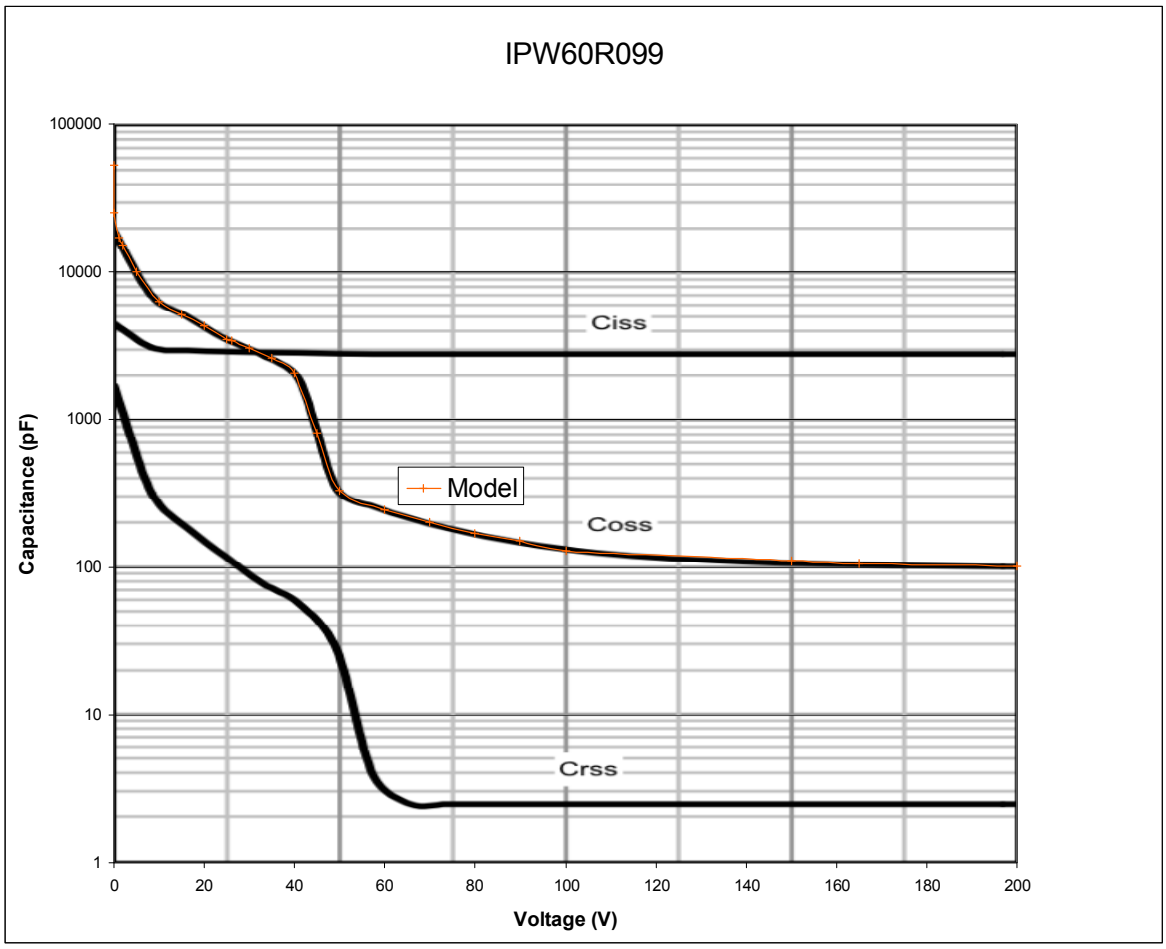


Figure 10-16: 20 Discrete points were fitted to the manufacturer-supplied C_{OSS} curve for the IPW60R099 silicon MOSFET

10.4.3 Numerical back-to-back blocking analysis

In the green region of Figure 10-14, the large phase is initially connected to the common node. The next major step in the switching sequence disconnects the large phase from the common node and connects to the medium phase instead. Throughout this transition, both transistors in the small phase leg remain switched off. Before the transition, the small pair of transistors blocks the large to small phase-phase voltage. After the transition, they block the medium to small phase-phase voltage which is of opposite polarity and smaller magnitude. In the green region of Figure 10-14, the large-small and medium-small voltages are 165V and -26V respectively. Figure 10-17 illustrates the pair of back-to-back transistors in the small phase leg as Q1 and Q2 before and after the transition. Because Q1 and Q2 remain off throughout the transition, they can be modelled by their voltage dependent parasitic output capacitances C(Q1) and C(Q2) using the voltage dependencies modelled in 10.4.2. The prototype cyclo-converter circuit also has 100pF ceramic

capacitors connected in parallel with each transistor's drain and source terminals which will be included in numerical calculations for C(Q1) and C(Q2).

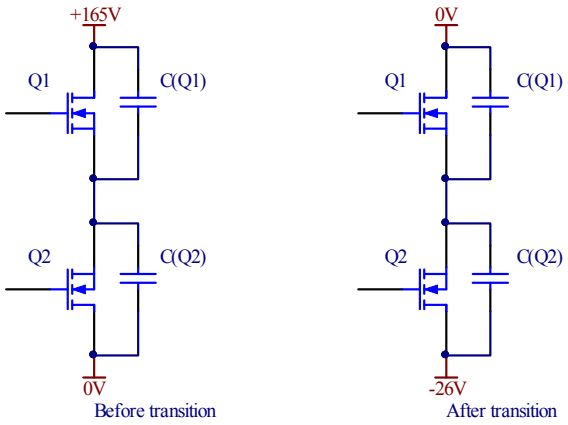


Figure 10-17: Voltages across a pair of back-to-back transistors before and after the transition

Before the transition, C(Q1) is charged to 165V. At 165V, an IPW60R099 MOSFET has an output capacitance of approximately 105pF (plus the parallel 100pF capacitor in the prototype power converter) and holds 33.8nC of charge. During the transition, current flows upwards through Q2 and Q1, discharging C(Q1) and charging C(Q2). If it is assumed that C(Q2) is charged to -26V, C(Q2)'s capacitance is approximately 3.6nF after the transition (including the parallel 100pF capacitor) and thus, stores 93.6nC. This is much larger than the charge that was stored by C(Q1) before the transition, proving that C(Q1) had to completely discharge during the transition and that some additional current flowed through Q1's body diode to allow C(Q2) to completely charge to 93.6nC. The body diode voltage drop across Q1 is typically 0.9V. The common node between Q1 and Q2 is at a potential of 0.9V after the transition and Q2 blocks 26.9V. The capacitance of Q2 at 26.9V is close enough to that at 26V to be assumed equal.

10.4.4 Parasitic winding capacitance

In the cyclo-converter prototype, the transistor gate drive circuits are powered from multiple windings of a flyback transformer. The inter-winding capacitance of this transformer was measured using a Wayne Kerr 3260B precision magnetics analyser and found to be 57pF ±0.1% at 100kHz and 53pF ±0.1% at 3MHz. The inter-winding capacitance is not believed to decrease significantly at high voltages, but a conservative 50pF has been used in numerical calculations. The inter-winding capacitance couples

between the common midpoint of each transistor pair and the mains. This effectively places the capacitance directly in parallel with one transistor from each pair, as demonstrated in Figure 10-18.

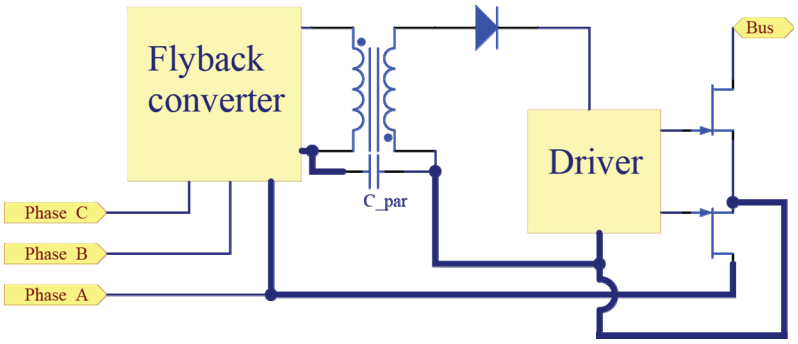


Figure 10-18: Parasitic capacitance of auxiliary supply transformer appears across the lower JFET

Note that the upper and lower transistors in Figure 10-18 are specific physical transistors that remain connected to their particular mains phase (phase A) at all times. Q1 and Q2 in Figure 10-17 are mapped onto different physical transistors for subsets of each 30° segment of the mains using the large/medium/small convention.

Figure 10-19 shows the transistors from Figure 10-17 during the portion of a mains segment where C_par is in parallel with Q1. The charge in C(Q1) and C_par before the transition was recalculated to include C_par and found to be 42.1nC. This is still much smaller than the 93.6nC that C(Q2) gains during the transition, so C(Q1) still experiences a full discharge. C_par , therefore, does not have a significant effect on the switching behaviour of the silicon MOSFETs.

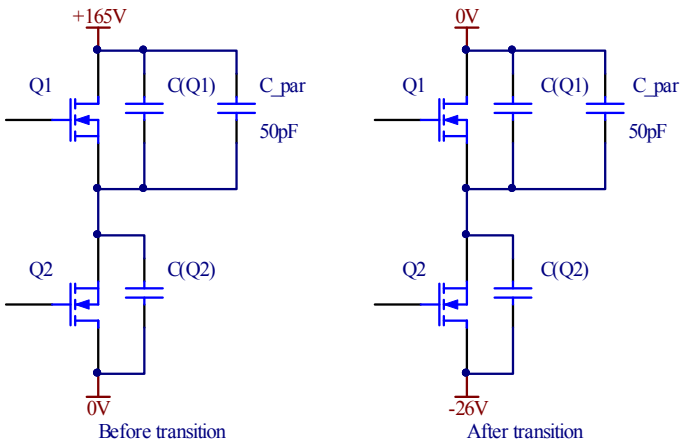


Figure 10-19: Small phase leg with parasitic capacitance across Q1

10.4.5 Switching behaviour with SiC JFETs

The parasitic winding capacitance has a more significant effect on the switching characteristics of the SiC JFETs than the silicon MOSFETs. At 165V, the SJEP120R125 has approximately 55pF (plus the 100pF external capacitor and 50pF inter-winding capacitance) and so $C_{(Q1)}$ stores 33.8nC of charge. After the transition, if it is assumed that $C_{(Q2)}$ is charged to -26V, Q2 has a capacitance of approximately 125pF and (with the parallel 100pF capacitor) stores 5.9nC of charge. This is less than the 33.8nC that was stored by Q1 and its parallel capacitances before the transition, indicating that C1 could not have been fully discharged. Instead, $C_{(Q1)}$ could only have been discharged by 5.9nC, resulting in some residual voltage left across Q1 disproving the assumptions about Q1's voltage after the transition. Q2 must block the sum of this residual voltage and 26V, so the assumptions about Q2's voltage and hence capacitance, after the transition, are also disproved. The correct solution can be found by performing a number of iterations on the circuit voltages and capacitances until convergence is achieved.

Using the mains voltages 6 degrees away from a magnitude crossing, the voltages and capacitances of Q1 and Q2 were calculated iteratively for both IPW60R099 silicon MOSFETs and SJEP120R125 SiC JFETs to solve for several different combinations of external parasitic capacitances. The calculations were based on the charge removed from Q1 and its paralleled capacitances being equal to the charge added to Q2 and its paralleled capacitances. The converged results of these iterative calculations are summarized in Table 10-4. No substantial effects were found with the silicon MOSFETs. However the asymmetric parasitic capacitance of the auxiliary transformer was found to significantly increase the residual voltage across Q1 with SiC JFETs.

Parallel device combination	**V_{Q1}**	**V_{Q2}**
IPW60R099 MOSFET + 100pF capacitor	0V	-26V
IPW60R099 MOSFET + 100pF capacitor + 50pF winding	0V	-26V
SJEP120R125 SiC JFET	20.0V	-46.0V
SJEP120R125 SiC JFET + 50pF winding	60.4V	-86.4V
SJEP120R125 SiC JFET + 100pF capacitor + 50pF winding	65.6V	-91.6V

Table 10-4: Iteratively calculated post-transition voltages 6 degrees away from a magnitude crossing.

At a magnitude crossing point, the peak large-small voltage of $120 \cdot \sqrt{3} \cdot \sin(60) = 180\,\text{V}$ occurs. At this point, the post-transition drain-drain voltage across the small phase (medium-small phase-phase) is zero due to the small and medium phase voltages intersecting. Iterative calculations were performed at this operating point and are summarized in Table 10-5. V_{Q1} and V_{Q2} are always equal and of opposite polarity at this point because of the zero post-transition drain-drain voltage.

Device combination	**V_{Q1}**	**V_{Q2}**
IPW60R099 MOSFET + 100pF capacitor	0V	0V
IPW60R099 MOSFET + 100pF capacitor + 50pF winding	0V	0V
SJEP120R125 SiC JFET	33.5V	-33.5V
SJEP120R125 SiC JFET + 50pF winding	75.9V	-75.9V
SJEP120R125 SiC JFET + 100pF capacitor + 50pF winding	84.1V	-84.1V

Table 10-5: Iteratively calculated post-transition voltages at a magnitude crossing.

10.4.6 Asymmetry of the back-to-back blocking behaviour

As a result of the small output capacitance of the SiC JFETs, the back-to-back blocking phenomenon occurs regardless of whether or not the parasitic 50pF of inter-winding capacitance is present. Iterative calculations were performed with the 50pF of inter-winding capacitance located in parallel to Q2 instead of Q1 (as occurs during a subset of a different mains segment). The results are shown in Table 10-6 with the 100pF capacitors included. In both cases the effect is reduced compared to that with the inter-winding capacitance across Q1.

Device combination	**V_{Q1}**	**V_{Q2}**
SJEP120R125 SiC JFET with 50pF winding capacitance across Q2, 6° from magnitude crossing	39.1V	-65.1V
SJEP120R125 SiC JFET with 50pF winding capacitance across Q2 at magnitude crossing	58.5V	-58.5V

Table 10-6: Iteratively calculated post-transition voltages with the 50pF parasitic capacitance in parallel with Q2 instead of Q1.

Other mains segments exist where the phenomenon would also be expected to take place through symmetry. However, in these segments the common node between the two JFETs

would need to be more positive than either drain. For this reason, they are not possible as a result of clamping by the JFETs' body diode-like characteristics. In these impossible regions, the effect would have been made larger by the addition of inter-winding capacitance across Q2. Therefore, under all circumstances that the effect can occur, adding extra capacitance in parallel with Q2 will reduce the size of the phenomenon.

To test this theory, capacitors were connected in parallel with each lower physical JFET in the prototype cyclo-converter. These three JFETs represent Q2 in regions where the phenomenon occurs and Q1 where it does not. The magnitude of V_{Q2} was measured at the point in the mains cycle highlighted green in Figure 10-14 and the results repeated with different capacitances. Iterative calculations were also performed for a range of capacitances and are shown alongside the measured results in Figure 10-20. 1nF of extra capacitance is sufficient to reduce the post-transition voltage of Q2 to less than 25V.

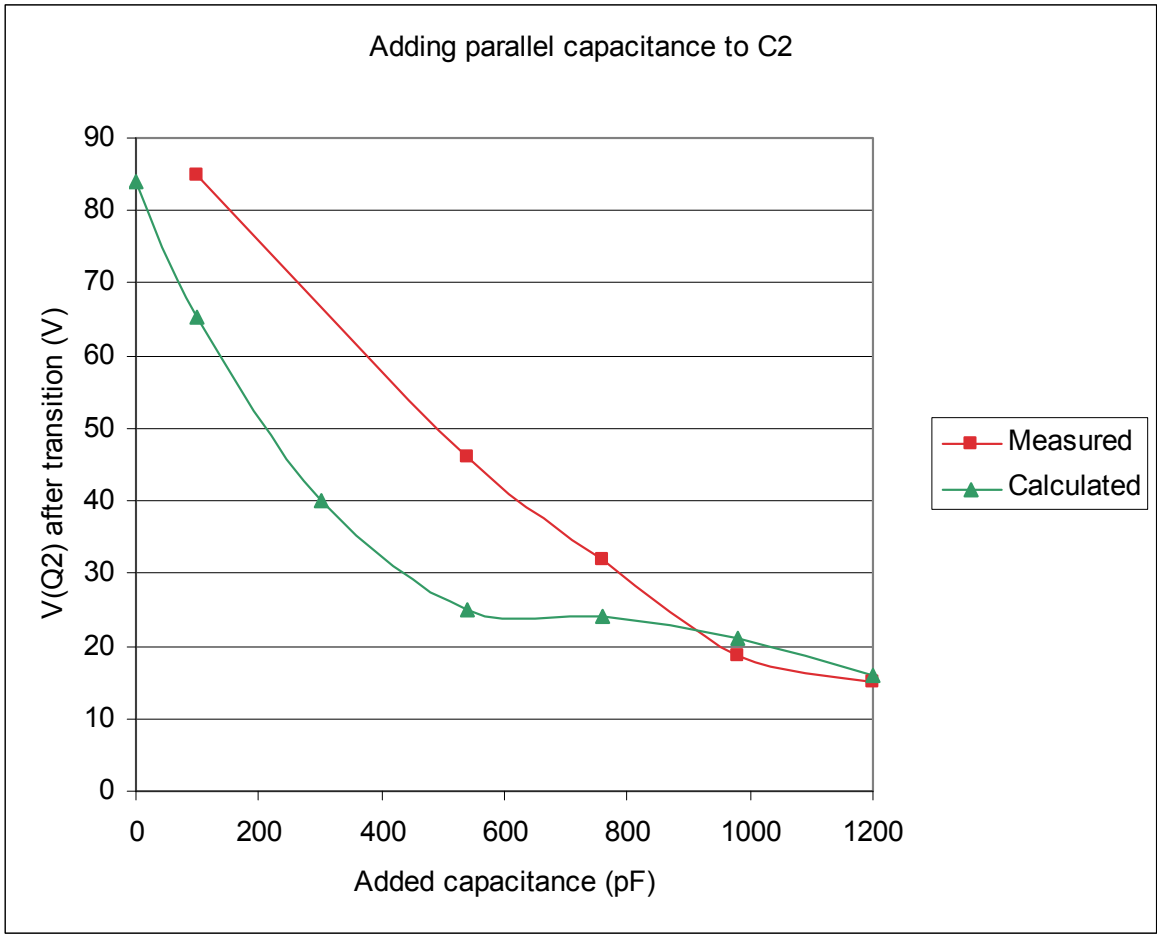


Figure 10-20: Adding capacitance in parallel to Q2 reduces the magnitude of the resulting Q2 voltage

The measured values for V(Q2) were notably larger for low values of added capacitance. This suggests that parasitic capacitances not included in the calculation such as those between traces on adjacent PCB layers, could be contributing to the phenomenon. The addition of capacitance across the lower JFET to reduce the voltage that it blocks only affects the current through the JFET during transients (where the turn-on energies are altered) and has no significant effect on the resonant tank current over a switching cycle. The cycloconverter is also immune to any symmetry changes caused by the addition of capacitance in parallel with the lower JFETs because the series resonant capacitor blocks any DC offset.

10.4.7 Consequences of back-to-back blocking

In the switching scheme employed by the prototype converter, the back-to-back blocking behaviour described in section 10.4 results in larger voltages being blocked by both SiC JFETs in each pair than would be blocked if silicon MOSFETs had been used. This increases the amount of stored energy in each transistor, but the prototype cyclo-converter switches its transistors on under zero voltage conditions so that the additional stored energy is unlikely to have any measurable effect on switching losses. However, the transistors must be able to handle any additional voltage or current stress that may occur.

The voltage blocked by Q2 after a transition increases with the size of $C_{(Q1)}$. The hypothetical worst case scenario is that $C_{(Q1)}$ has infinite capacitance. This would cause the voltage across C1 to remain the same throughout the transition. Q2 blocks the sum of V_{C1} and the drain-drain voltage post-transition. V_{C1} is the difference between the large and small phases V_L-V_S. The post-transition drain-drain voltage is the difference between the medium and small voltages V_M-V_S. Therefore, the voltage that Q2 blocks post-transition with an infinitely large C1 is the large-medium voltage, as shown in *Eq 10-35*. This is exactly the peak phase to phase voltage already withstood by any transistor in the cyclo-converter when its leg is the medium or large leg. Thus, the back-to-back blocking phenomenon poses no larger voltage stress on any transistor than is already present.

$$\left|V_L - V_S\right| - \left|V_M - V_S\right| = \left(\left|V_L - V_S\right|\right) - \left(V_M - V_S\right) = V_L - V_M \qquad \textit{Eq 10-35}$$

This property can also be seen elegantly in Figure 10-21 where the voltages across the infinitely large $C_{(Q1)}$, the voltage across the bridge-leg after the transition and the voltage across Q2 post-transition are shown, represented by $|V_L-V_S|$, $|V_M-V_S|$ and $|V_L-V_S|+|V_M-V_S|$ respectively. The voltage blocked by Q2 in this case follows the same envelope as a three-phase rectifier.

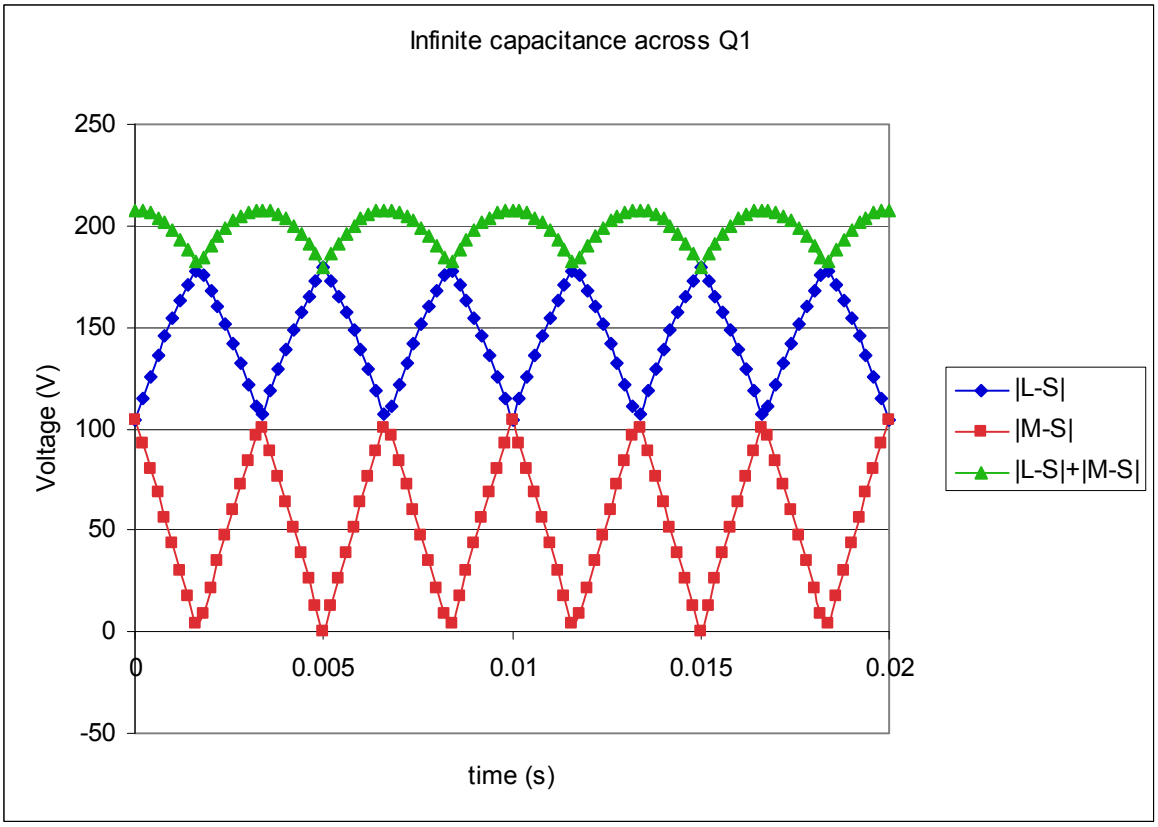


Figure 10-21: Voltages across Q1 (blue), the bridge-leg (red) and Q2 (yellow) after a large to medium transition with infinite $C_{(Q1)}$

The actual voltage stresses experienced by the SiC JFETs are lower than the worst case scenario. With the 100pF parallel capacitors and 50pF of parasitic winding capacitance, the post-transition voltage of Q2 was computed iteratively at a number of operating points using the capacitance models from section 10.4.2 for both the SJEP120R125 SiC JFET and the IPW60R099 silicon MOSFET.

The operating points were evenly spread every 0.2ms over a single 50Hz mains period with the results shown in Figure 10-22. With silicon MOSFETs, the post-transition voltage across Q2 is only slightly (Q1's body diode forward drop) larger than the drain-drain voltage across the pair of MOSFETs. The SiC JFET at the same set of operating points blocks significantly more voltage.

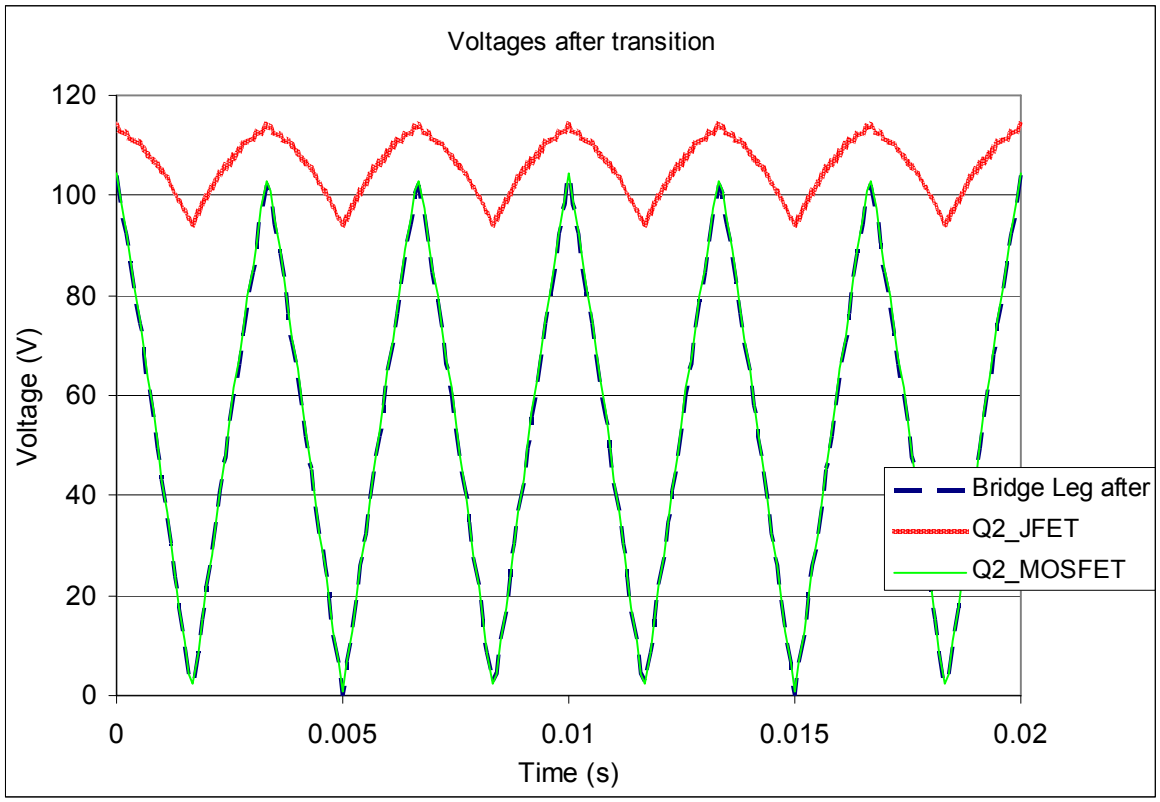


Figure 10-22: Bridge and Q2 voltages in the small phase after the transition

Although the prototype converter achieves lossless ZVT turn-on, minimizing any effects of increased energy storage in Q2's output capacitance, it is of academic interest to calculate this energy storage.

Energy calculations were performed on the data points in Figure 10-22 with the results shown in Figure 10-23. The average stored energy was 710nJ for an IPW60R099 silicon MOSFET and 774nJ for a SJEP120R125 SiC JFET. The SiC JFETs have only 9% more stored energy on average, despite the squared relationship between voltage and energy in a capacitor, because the output capacitances of the SiC JFETs are so much smaller than those of the silicon MOSFETs.

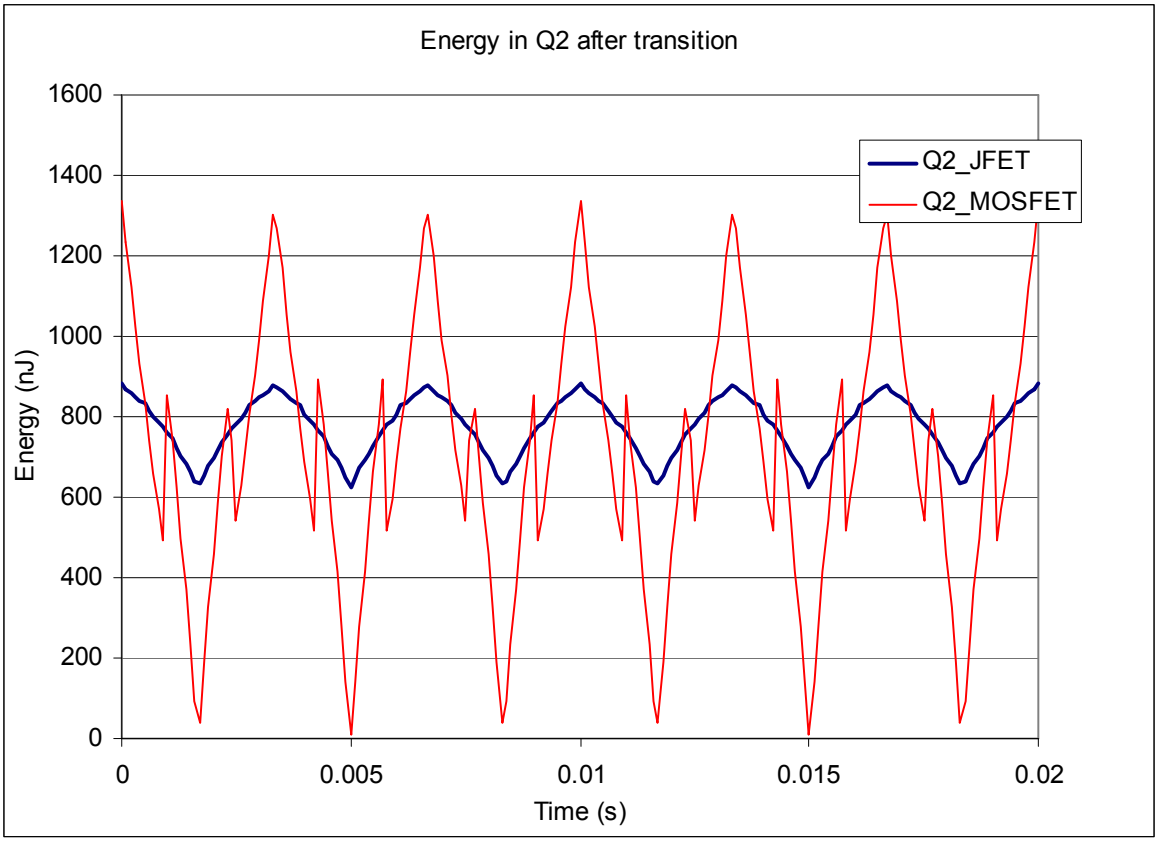


Figure 10-23: Stored energy in Q2 after transitioning

Although it is possible to reduce the magnitude of the phenomenon by adding capacitance in parallel with each of the three upper transistors, there is no benefit in doing so because the phenomenon does not cause any significant performance degradation. The additional 9% stored energy in Q2 when using SiC JFETs compared to silicon MOSFETs is unlikely to have a significant effect on losses in a soft-switched converter. In a hard-switched converter, the 64nJ could be dissipated as heat, increasing losses. At a switching frequency of 100kHz, the absolute increase in losses would be 6.4mW per phase, substantially smaller than any difference between the SiC JFETs' and silicon MOSFETs' drive or conduction losses.

The back-to-back blocking phenomenon observed does not necessarily apply exclusively to SiC JFETs: If silicon MOSFETs with similar output capacitance characteristics to the SiC JFETs are developed, the same effect will be observed. Knowledge of the phenomenon is novel and considered of value to designers of any power converter that uses one or more pairs of SiC JFETs connected source to source. Subsequently, an overview of the phenomenon was published by the author in [9].

10.5 Cyclo-converter Efficiency tests

10.5.1 Test methodology

One of the most important performance metrics for the cyclo-converter is conversion efficiency. Power flowing into the cyclo-converter was measured using a calibrated Yokogawa PM3000A power meter. The meter was configured in four-wire mode where two parallel voltage sensing connections and a separate series current sensing loop are used for each phase to correctly exclude cabling losses. The power meter is able to measure real power flow in all three phases simultaneously and display their sum with an error of ±0.12% of the reading ±0.6mW.

The output power of the cyclo-converter was measured using a pair of HP34401A high precision multi-meters. These calibrated meters offer basic DC accuracy of 0.0035% [131]. One meter was used to sense output voltage directly at the power converter's output connector. The other meter measured the voltage drop across a calibrated 0.25mΩ shunt. The shunt was forced-air cooled to minimize drift.

At each measurement point, the converter was allowed at least three seconds to settle. If the input power or transistor temperature was still visibly changing, additional settling time was allowed to achieve steady state operation. The power meter and two multi-meters were read simultaneously using their hold functions. Three measurements were taken and averaged at each operating point to further boost accuracy.

The latest revision of the cyclo-converter prototype uses the latest IPW60R045 MOSFETs, which exhibit lower on-resistance than those used in the back-to-back blocking analysis. To better compete with the advances in silicon MOSFET technology occurring during the course of the research, the latest SJEP120R100 normally-off SiC JFETs from SemiSouth were used in the SiC version. These JFETs offer lower on-resistance than their SJEP120R125 predecessors that had been used during the functional development and testing of the cyclo-converter.

10.5.2 Results

The switching characteristics of the SiC JFETs are very different to those of the silicon MOSFETs that the cyclo-converter typically uses. This caused a significant timing

mismatch between the JFETs and the synchronous rectification (SR) MOSFETs on the output of the converter. The problem can be solved by extensive recalibration of the SR timing in software to match the SiC JFET characteristics. This product development task is beyond the scope of this study. Instead, the SR functionalities on both the SiC JFET and silicon MOSFET based cyclo-converter prototypes were disabled to provide a fair test, albeit with lower overall converter efficiency for both converters. The SiC JFET based cyclo-converter was operated in small load steps up to 1.45kW. Increasing the load beyond 1.45kW resulted in a rapid increase in forward voltage drop across the SiC JFETs, leading to a decrease in output voltage that, in turn, triggered the converter's protection circuitry. The problem was reproduced several times at power levels that occurred consistently within 50W of each other. The test procedure was repeated with a silicon MOSFET based prototype cyclo-converter and the results of both tests are shown in Figure 10-24.

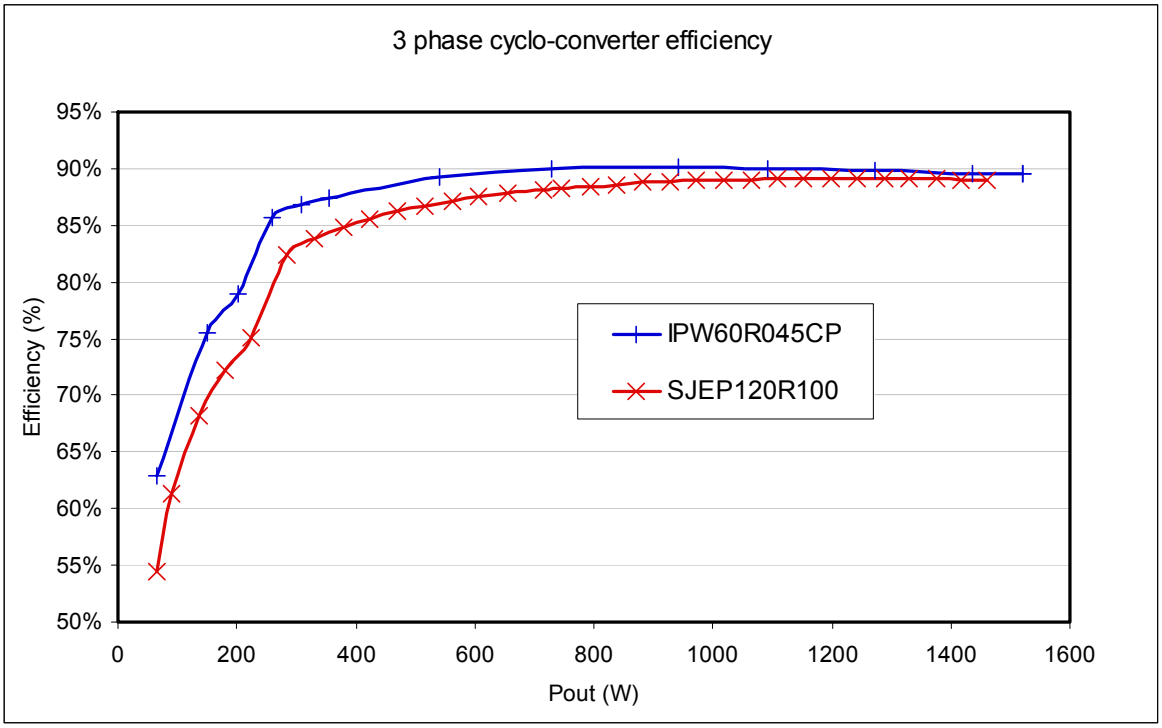


Figure 10-24: Cyclo-converter efficiency with synchronous rectification disabled

The efficiency of the two converters converges with increasing load, suggesting that the SiC JFETs exhibit smaller conduction losses but larger standing losses. Figure 10-25 shows the losses in each converter. At a load of 1.4kW, the difference is less than 10W. Savings of several Watts could be made by redesigning the gate drive circuits to better suit the 1200V SiC JFETs, potentially bringing the JFET converter efficiency very close to or potentially above that of the 600V silicon MOSFETs. It is interesting to note that the rated

$R_{DS(on)}$ of the SJEP120R100 SiC JFETs is more than double that of the IPW60R045, yet the apparent trend indicates better conduction in the SiC JFETs.

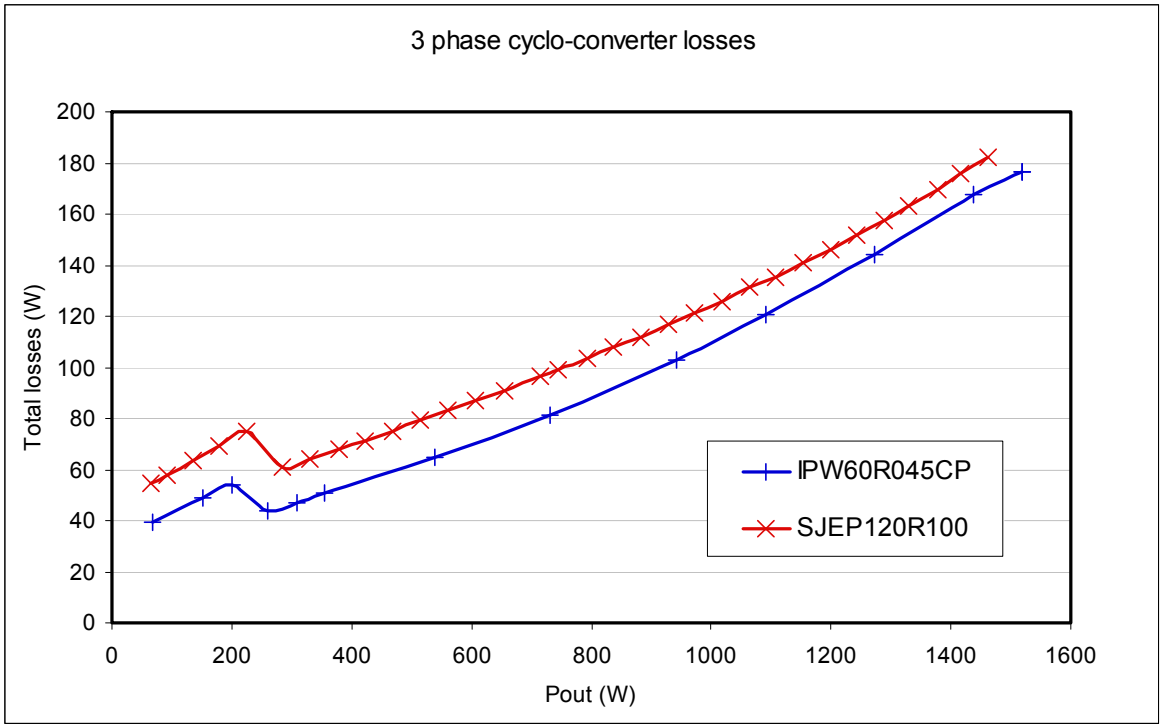


Figure 10-25: Losses in the three phase cyclo-converter

The cycloconverter was able to operate up to a load of 1450W with the EM SiC JFETs. Above this level, the cycloconverter' protection circuitry was triggered. The peak current through the resonant tank was approximately 16A which is within the SJEP120R100's 125°C rating of 17A. The junction temperatures of the JFETs can be shown to be less than 125°C by considering their junction to case thermal impedances, the total circuit losses and the maximum measured case temperature of 48.3°C.

10.5.3 Higher voltage cycloconverters

In a higher voltage cyclo-converter designed for a 400V or 415V power system, 600V silicon MOSFETs cannot be used. This is because each transistor needs to be capable of blocking the peak phase to phase voltage under worst case conditions with a safety margin. The nominal peak phase to phase voltage for a 415V system is $415 \cdot \sqrt{2} = 587\,\text{V}$. Typical safety margins and mains tolerances of 20% and 15% respectively dictate that a device rating of at least 810V is required. 900V silicon MOSFETs are therefore a reasonable choice in such an application. The lowest $R_{DS(ON)}$ typically found in 900V silicon

MOSFETs is around 120mΩ, higher than that of the SiC JFETs. 900V silicon MOSFETs also exhibit poorer switching performance than their 600V counterparts. Hence, it is hypothesized that the 1200V SiC JFETs will outperform 900V silicon MOSFETs in a 400V or 415V three phase cyclo-converter and should be evaluated for such an application.

The resonant switching in this topology results in very low switching losses that are expected to remain relatively small in a 400V or 415V version. Meanwhile, the increase in input voltage will cause a reduction in the current through the JFETs at any particular power level, resulting in smaller conduction losses in proportion to the square of the voltage ratio. If it is assumed that there is an equivalent of 11.3A RMS flowing through two series conducting JFETs in the 208V version at 1350W load, the conduction losses with a channel resistance of 100mΩ, the estimated conduction loss is 25.6W. Increasing the line to line voltage from 208V to 415V should lead to a current of 5.7A RMS through the JFETs. This results in a conduction loss of 6.4W, a 75% reduction. This is equivalent to an improvement in converter efficiency of 0.14%. If a channel resistance of 140mΩ is used to incorporate the elevated junction temperature, the efficiency improvement increases to 0.20%. In practice, the junction temperature would be lower in the 415V converter than the 208V converter due to the reduced conduction losses, further increasing the improvement. These values are provided as indicative estimates and should not be considered accurate predictions.

10.6 Conclusions

A three-phase cycloconverter was retrofitted with EM SiC JFETs and operated with a load of 1450W. At 1400W, the losses were within 10W of those exhibited when the cycloconverter was fitted with 600V Si MOSFETs. Unique switching behaviour was observed with SiC JFETs that had not previously been seen in the literature. The phenomenon was explained by the SiC JFETs' output capacitance varying significantly with voltage. The phenomenon was shown to not pose any greater voltage stress on the JFETs than would normally be experienced in this topology.

The EM SiC JFET should be considered as a potential candidate in future 400V and 415V cycloconverter products.

Chapter 11 Conclusions

11.1 Future work

The SiC JFETs produced by SemiSouth have a blocking voltage of 1200V. Single-phase mains applications, where voltages of less than 600V need to be blocked, fail to fully utilize this feature of the SiC JFET. As a result, slightly better performance is often achieved by 600V silicon MOSFETs than 1200V SiC JFETs.

Higher voltage applications are better able to realise the potential of the 1200V SiC JFET. 400V and 415V three-phase applications are of particular interest as they utilize a larger portion of the 1200V capability. In these applications, 900V silicon MOSFETs are typically used. Testing in the PFC circuit in Chapter 8 and the commercial telecommunications rectifier in Chapter 9 already indicate that 1200V SiC JFETs perform better than 900V silicon MOSFETs in some scenarios. It is highly likely that 1200V SiC JFETs will allow higher electrical efficiency and/or switching frequencies to be achieved than 900V silicon MOSFETs. The three-phase cyclo-converter is a topology that is likely to achieve particularly good electrical efficiency with SiC JFETs. Higher voltage applications are even more likely to benefit from the use of SiC JFETs. The significance of the potential to switch faster than 900V Si MOSFETs in three-phase applications should not be underestimated. The associated decrease in the physical size of the passive components could substantially increase the power density of the end product, in turn reducing manufacturing costs. As the price of silicon carbide devices is driven down by maturing technology, increased competition and economies of scale, the price premium for silicon carbide over silicon could be recouped or exceeded by the saving associated with a higher power density product.

In addition to the finding that 1200V SiC JFETs achieve similar performance to 600V Si MOSFETs when implemented as a drop-in replacement in a commercial telecommunications power supply, it should be noted that the gate drive circuit in this supply was heavily optimized for Si MOSFETs. The conversion efficiency achieved with SiC JFETs could be improved further by redesigning the drive circuitry to better suit SiC JFETs. In particular, the use of a 13V supply to drive a sustained gate current through the SiC JFET with a gate-source voltage of 3V means that a majority of the drive power was

wasted in the drive circuit. As described in section 9.3.4, savings of approximately 1.5W could be made by redesigning the auxiliary power supply to deliver a more appropriate output voltage. This saving is similar in magnitude to the difference in overall efficiency observed between the SJEP120R100 SiC JFET and the FCH35N60 in the commercial telecommunications rectifier. It is also worth investigating whether it is possible to change the manufacturing process for SiC JFETs to achieve more favourable conduction and/or switching characteristics at the price of a lower blocking voltage. For example even if the blocking voltage of the SiC JFET had to be reduced by 30% to achieve only a 15% better $R_{DS(on)}$, the resulting device would still likely outperform both 600V and 900V Si MOSFETs in many applications.

The work covered between Chapter 6 and Chapter 8 has opened up a number of possibilities for future work. The PI control circuit described in Chapter 8 was not able to adequately regulate the output voltage of the PFC circuit over a wide operating range without suffering from oscillation at higher input voltages. A controller with a dynamic gain response should be investigated, specifically where the gain of the controller is decreased with increasing input voltage. This would help to mitigate the effects of the converter's plant gain which decreases substantially with increasing input voltage through the DCM range. A digital controller is recommended for more easily implementing this functionality.

Another opportunity for further development is the modification of the PFC circuit in Chapter 6 to achieve zero voltage transitions. This is recommended because the SiC JFETs exhibited good switching speeds in this application and a redesign for ZVT could improve the efficiency further by reducing the turn-off losses.

A particularly promising opportunity for further work on the PFC circuit in Chapter 6 to Chapter 8 is the implementation of a peak current controller. Under peak current control, the on time of the low side transistor is controlled by monitoring the rising inductor current. When the inductor current reaches the desired threshold the transistor is turned off for the rest of that particular switching cycle. The peak current setpoint would be controlled by a second, much slower control loop to achieve output voltage regulation. The use of peak current control should solve the stability issues experienced in Chapter 8 by keeping the peak current similar over consecutive switching cycles. Peak current control

can readily be extended to achieve valley switching by monitoring the bridge voltage to detect valleys and turning on the transistor at the bottom of a valley. A consequence of combining these two strategies is that the switching frequency will no longer be constant. As long as the switching frequency is maintained within a suitable range, this should not significantly impact other aspects of the circuit.

The practical implementation of the PFC converter described in Chapter 7 could also be improved. In particular, a four or six layer PCB should be considered, potentially with thicker copper layers. This would allow for lower impedance connections to be made, more flexible routing and more continuous ground planes. Surface mount ICs are also available containing hall-effect devices for current measurement. These could facilitate current measurements for both the proposed peak current control scheme as well as general circuit characterization without introducing as much parasitic inductance as the wire loops used in Chapter 7. The use of high voltage surface mount capacitors should also be considered in addition to the existing film capacitors as a potential method for achieving more localized decoupling.

Other SiC transistor technologies should also be considered, particularly a number of new devices that have emerged during the course of this research. SemiSouth have recently released the SJEP120R100 SiC JFET, adopted in the final parts of this thesis, as a superior replacement for the SJEP120R125. Transic developed a 50A SiC BJT[102] that should be evaluated for applications where the current carrying capacity of the SJEP120R100 is insufficient, for example in a 5kW, 415V three phase cyclo-converter. It may be possible to develop a normally-off SiC JFET that trades some of its blocking voltage for sufficient improvements in $R_{DS(on)}$ and/or switching speed to make it an attractive alternative to 600V Si MOSFETs. It is therefore recommended that if SemiSouth (or any other manufacturer) produces a normally-off SiC JFET with a blocking voltage of less than 1200V that it be evaluated for use in single phase applications.

Another SiC device that has recently been developed is a 33A, 1200V SiC MOSFET manufactured by Cree. The MOSFET has a $R_{DS(on)}$ of 80mΩ [73] and could be a potential substitute for 900V silicon MOSFETs. Major improvements have been made to overcome historic problems with SiC MOSFETs such as time dependant dielectric breakdown [68,

132], though there are still some outstanding issues regarding threshold voltage stability [133].

Following the recent closure of SemiSouth Inc [101], it is expected that normally-off SiC JFETs are less likely to have a significant role in telecommunications power converters over the next few years than other devices. The significant developments that have been made in SiC MOSFET technology over the last few years make these devices one of the more likely candidates for telecommunications power converters in the near future. Meanwhile, the number of commercial entities involved in the development of normally-on SiC JFET technology suggests that this too could be a worthwhile area to consider for future telecommunications power converter research. By the end of the research in this thesis, SemiSouth were already producing normally-on SiC JFETs with significantly lower $R_{DS(on)}$ values than their own normally-off JFETs, allowing these devices to already potentially outperform 600V silicon MOSFETs.

Although there has been reluctance to adopt normally-on transistors into commercial telecommunications power converters as a result of concerns about fault conditions, there is significant literature on the mitigation of these issues. The cascode connection is one particularly promising option. Infineon has also indicated, in a private communication, that it plans to announce a new normally-on SiC JFET in the near future as well as a dual driver IC capable of directly driving both a normally-on SiC JFET and a series-connected low voltage MOSFET to achieve a normally-off characteristic [134].

Ultimately, the fight between SiC MOSFETs and normally-on SiC JFETs comes down to commercial risk perception. Specifically, the risks associated with gate oxide reliability and the use of normally-on devices as well as their price premium will need to be outweighed by the advantages of SiC devices over Si before widespread adoption will occur. This is perceived as being something that will occur gradually over time rather than a step change associated with any particular event. Simplification of the drive circuitry for SiC devices is another area that will help reduce the barriers for adoption into commercial products. Both the use of a charge-pump to achieve a self-contained negative supply rail for the driver circuit as proposed in Chapter 5 and the Cissoid Atlas driver IC [114] are examples of major steps towards minimizing the role that driver circuitry plays in the decision making process for power converter switches.

Another area of development in high bandgap devices that should also be noted is that of GaN JFETs. While SiC devices possess very large blocking voltages that make competing with the 600V Si MOSFETs in existing products on a $R_{DS(on)}$ basis challenging, GaN transistors tend to exhibit excellent $R_{DS(on)}$ but fail to compete with 600V Si MOSFETs due to their insufficient blocking voltages. Just as the $R_{DS(on)}$ of SiC JFETs is falling, the blocking voltage of GaN JFETs is rising. Thus, 600V Si MOSFETs have the potential to be cannibalized from both sides by these competing technologies. In the shorter term, the output stages of telecommunications power converters where synchronous rectification of the 48V DC output occurs is likely to be the firs area where GaN devices are deployed. Here, much lower blocking voltages are required, although the $R_{DS(on)}$ of silicon devices is also much lower. As silicon MOSFETs continue to mature alongside SiC and GaN devices, it is conceivable that in the near future to achieve the highest possible efficiency in a telecommunications power converter, there may need to be SiC transistors in the PFC stage, silicon MOSFETs in the DC-DC stage and GaN transistors for synchronous rectification at the output. This underscores the rapidly changing technology in this field and the wealth of opportunities for further research.

11.2 Final Remarks

The telecommunications power converter market is consistently demanding higher and higher electrical efficiency. Several SiC transistors were considered as candidates for improving electrical efficiency in telecommunications power converters and two normally-off SiC JFETs from SemiSouth were evaluated for a broad range of topologies.

Unique characteristics of the normally-off SiC JFET were discovered that had not previously been described in the literature. These unique characteristics, as described in this thesis, have a significant impact on the drive losses in synchronous rectification applications and will adversely affect the performance of a power converter if one is uninformed about their consequences when designing SiC JFET gate drive circuitry. With knowledge of the effects, simple measures can be taken to achieve a better driving arrangement that significantly reduces drive losses without adversely affecting conduction losses.

A power factor correction circuit was constructed with SiC JFETs using a topology that cannot be constructed from 600V silicon MOSFETs because of their inadequate voltage rating. The 1200V SiC JFETs were found to perform well in this topology and to allow significantly higher switching frequencies to be achieved than possible with 900V silicon MOSFETs. The efficiency of the circuit was high, but did not rival that of alternative power factor correction topologies that are able to utilize 600V silicon MOSFETs. A fourfold improvement in switching speed is expected to enable this topology to achieve better electrical efficiency than that of the best existing power factor correction circuits. Alternatively, the modification of this topology to operate with zero-voltage transitions might also achieve the required reduction in switching losses needed to create the most efficient power factor correction circuit.

A commercial telecommunications power converter was modified to use normally-off SiC JFETs in its power factor correction circuit. Similar electrical efficiency was measured with 1200V SiC JFETs, to that with 600V silicon MOSFETs. 1200V SiC JFETs achieved better efficiency in this application than 900V silicon MOSFETs. The test used a simple modification of the power converter product to incorporate SiC JFETs. A complete redesign of the gate drive circuitry would allow the 1200V SiC JFETs to achieve an even closer efficiency to that of the 600V silicon MOSFETs.

A 208V three-phase cyclo-converter was modified to accommodate 1200V normally-off SiC JFETs. The converter was able to successfully operate at up to 60% its maximum rated load and achieved an electrical efficiency within 0.8% of that achieved with the best available 600V silicon MOSFETs. When 400V and 415V versions of this converter are produced, they are expected to be capable of operating at full load with 1200V normally-off SiC JFETs and are expected to achieve higher conversion efficiency than with 900V silicon MOSFETs.

Unique switching characteristics were identified in the cyclo-converter that occur as a result of the significantly lower output capacitance of the SiC JFETs compared to that of silicon MOSFETs. These characteristics were not previously covered in the literature and contribute valuable insights to the field. Knowledge of these characteristics is of immediate value when designing power converters that utilize one or more pairs of normally-off SiC JFETs connected back-to-back. The phenomenon also applies to some silicon MOSFETs,

but not to a sufficiently significant degree to gain the attention of power converter designers. As advances in silicon MOSFET technology lead to the development of MOSFETs with lower and lower output capacitances, the phenomenon will become more significant. It was proven that the switching phenomenon cannot cause voltage stresses beyond those normally experienced in such applications and consequently is not a cause for concern.

The findings in this thesis demonstrate that the 1200V normally-off SiC JFET allows similar performance to be achieved to that possible with the best 600V silicon MOSFETs, whilst also offering twice the blocking voltage. This makes it a viable alternative to silicon MOSFETs in applications where voltages in excess of 600V must be blocked, and a close second to the 600V silicon MOSFET in many lower voltage applications.

Chapter 12 References

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Appendix A. Cascode connection of SiC BJT

The cascode connection is seen as a way to achieve optimal switching speeds with SiC BJTs because it diverts load current through the collector-base junction, effecting rapid injection and removal of charge.

To evaluate the performance of the cascode connection, three prototype circuits were designed.

1. Cascode test circuit

The first prototype circuit is a simple cascode connection where a low voltage silicon MOSFET is used to switch a high voltage BJT as shown in Figure A-1.

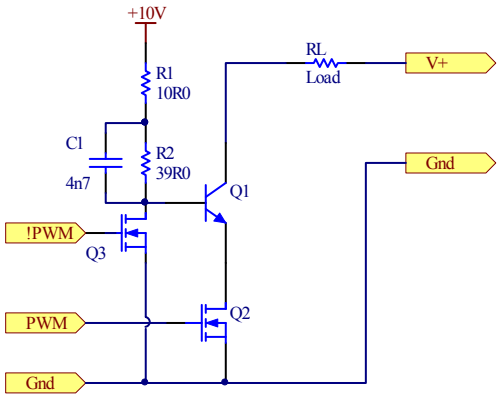


Figure A-1: Cascode test circuit with the BJT, Q1 in cascode with low voltage MOSFET Q2.

A PWM signal is applied to Q2 via a MOSFET driver. When Q2 turns on, the emitter of Q1 is grounded and Q1 receives a base current from the 10V supply via R1 and R2. To increase the turn-on speed, C1 allows a larger base current to flow initially.

When Q2 is turned off, the emitter voltage of Q1 rises until it is close enough to Q1's base voltage for Q1 to turn off. The load current briefly flows into Q1's collector and out of its base via R1 and R2 into the 10V supply, causing the rapid removal of charge carriers from the BJT junction. C1 provides a temporary low impedance path for this current as well as a charge-pump effect, improving the turn-off time of Q1. It is also possible to turn Q3 on when Q2 is turned off. This grounds the base of Q1 potentially allowing a larger collector-

base current to flow and therefore a faster turn-off time. It also reduces the voltage that must be blocked by Q2 because the base of Q1 is closer to ground than 10V.

The choice of MOSFET for Q2 is important as Q2 must conduct the full load current. This means that a low on resistance is highly desirable and that the device needs to be rated for operation at the full load current. The BitSiC 1206 has a maximum continuous current rating of 6A [75], dictating that the MOSFET chosen must also meet this requirement. When Q2 is off, it blocks approximately the BJT base voltage with respect to ground, about 10V in this prototype. It is inevitable that parasitic elements will cause the instantaneous voltage across the MOSFET to briefly be larger than this figure. A 30V MOSFET was therefore chosen to allow a wide safety margin.

In addition to these constraints, the parasitic capacitances of Q2 should be minimized to achieve the best possible switching speed. Ultimately the Infineon BSO300N03S MOSFET was chosen. It has a steady state current limit of 5.7A based on power dissipation. [135] Although the test application will see a load of 6A, the duty cycle is 50% and forced-air cooling is used, introducing ample derating to the 5.7A rating. The BSO300N03S has a $R_{DS(on)}$ of 30mΩ at 70°C which equates to a 180mV drop at 6A. This is insignificant compared to the saturation voltage of the BitSiC 1206 which is approximately 1.5V at 6A.

Q2 is a low side switch, allowing a standard MOSFET driver IC to be used. The UCC37322 was chosen for this task due to its extremely low output impedance of 15Ω when sourcing and 1.1Ω when sinking current, as well as its rapid transition times of 20nS into a 10nF load. [136]

To increase flexibility, another BSO300N03S, Q3 was connected across the base-emitter junction of the BJT, so that the junction could be short circuited during turn off, potentially offering a speed increase. This MOSFET floats at the emitter potential and was driven by the high side output of an integrated high and low side MOSFET driver.

The complete cascode drive circuit prototype is shown in Appendix B, Schematic 7 including decoupling capacitors and housekeeping circuitry.

2. Cascode connection with proportional drive

One of the caveats to the cascode connection is that a similar sized base current flows with both small collector currents and large. The base current, controlled by R1 and R2 in Figure A-1, must be large enough to achieve a small $V_{CE(sat)}$ at large collector currents for conduction losses to be acceptable. At light loads, when the collector current is small, such a base current is excessive and represents a waste of drive power.

One variation of the cascode connection involves the addition of a proportional drive component to the base current of the BJT. This causes the BJT to receive a larger base current when larger collector currents are being carried, ensuring a low $V_{CE(sat)}$ while conserving drive power at light loads.

A base current in proportion to the collector current can be easily achieved through the use of a current transformer as shown in Figure A-2.

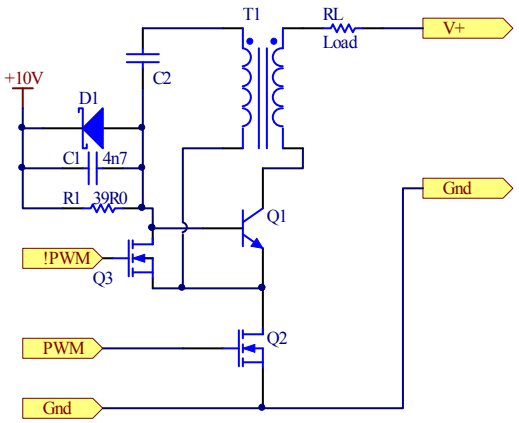


Figure A-2: The addition of current transformer T1 provides a base current in proportion to collector current

The turns ratio of T1 is designed to roughly match the current gain of Q1. An exact match is not possible as the current gain varies with current, temperature and from one physical transistor to another. In practice, a turns ratio that is too large will result in insufficient base current being delivered, relying more heavily on the 10V supply. Conversely a turns ratio that is too small will cause excessive base current to flow, increasing the current that D1 and/or Q3 must carry at turn-off.

Experimentation led to the selection of a 5:1 turns ratio. This ratio causes the base current to be slightly larger than necessary over a broad range of collector currents. When DC blocking capacitor C2 was replaced with a short circuit, it was found that the net power supplied from the 10V rail was negative for a broad range of duty cycles.

This allowed the 10V supply to be removed and replaced with a large capacitor and zener diode, simplifying the drive circuitry. Turning on Q3 was also found to be unnecessary during this mode of operation, resulting in Q2 being the only actively driven transistor as shown in Figure A-3. Thus an elegant solution was reached where a standard single-ended MOSFET gate driver IC can be used to switch Q2 and therefore Q1.

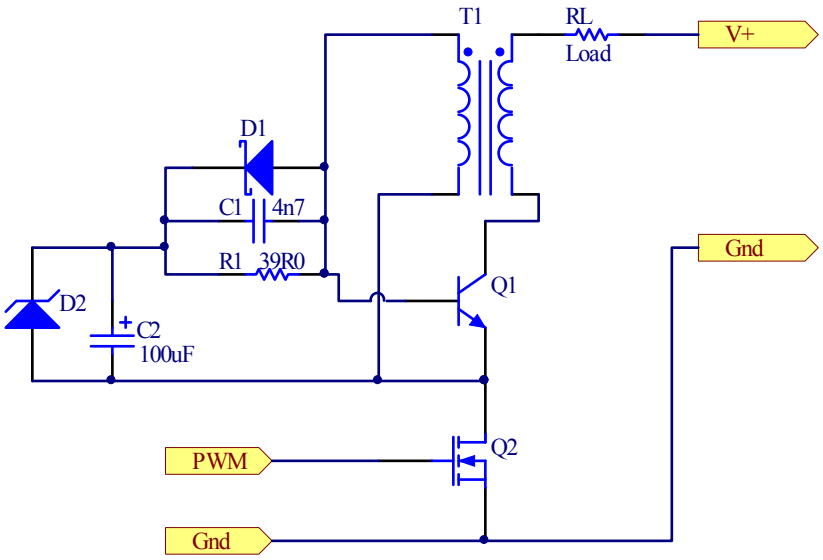


Figure A-3: Cascode connection with self-powered proportional drive

The complete self-powered cascode prototype circuit with proportional drive is shown in Appendix B, Schematic 8 with decoupling capacitors and housekeeping circuitry.

3. Non-cascode comparison

To create a benchmark against which to evaluate the cascode connection (with and without proportional drive) of a SiC BJT, a non-cascode drive circuit was designed. A low output impedance drive stage was constructed from a MOSFET half bridge as shown in Figure A-4 and connected to the BJT via a network consisting of R1, R2 and C1.

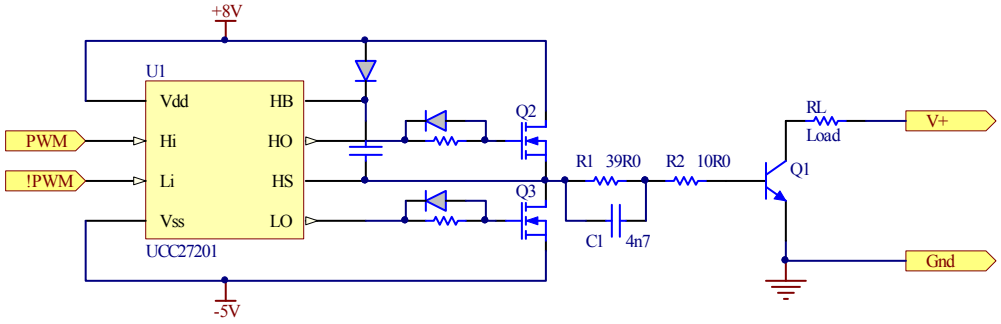


Figure A-4: Non-cascode comparison circuit

R1 and R2 together limit the sustained base current that flows through the BJT, while R2 and C1 set the peak current pulse and its shape at turn-on and turn-off instants to ensure that charge carriers are injected and removed from the BJT's base-emitter junction as rapidly as possible.

The complete non-cascode comparison circuit, including decoupling capacitors and housekeeping circuitry, is shown in Appendix B, Schematic 9.

4. Cascode circuit performance

In preparation for testing of the BitSiC1206 SiC BJT from Transic, the cascode circuits were tested with a BUF420 silicon transistor. The rise and fall times of the collector-emitter voltage were measured with all circuits configured as 60V to 30V buck converters. The rise and fall times observed are summarized in Table A-1.

	Simple cascode	Cascode with proportional	Non-cascode
Rise time	20ns	20ns	65ns
Fall time	30ns	50ns	70ns

Table A-1: Comparison of collector-emitter voltage rise and fall times

The cascode circuit offers a significant improvement in switching speed over the non-cascode comparison circuit. Despite extensive fine tuning, it was not possible to achieve faster switching with a proportional drive than without. It was noted that, with a larger than optimum turns ratio, the circuit could be operated from a proportional drive alone, without the need for a DC supply to bias the BJT.

The switching waveforms for the BUF420 switching at 500kHz are shown in Figure A-5. Some overshoot occurs at turn-off, causing ringing.

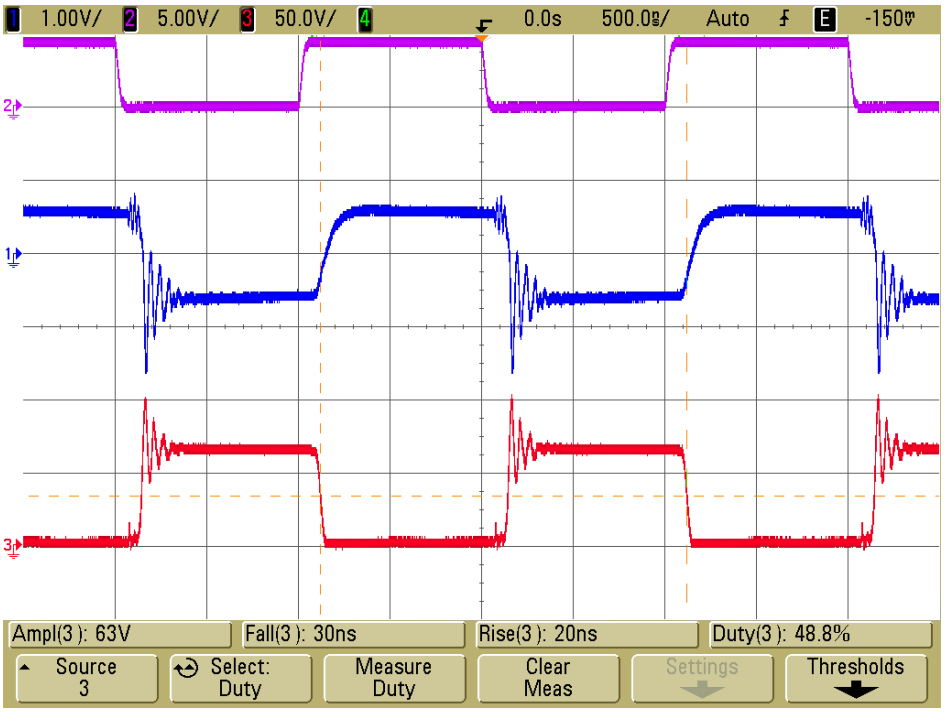


Figure A-5: Logic input (upper), collector current (middle) and collector-emitter voltage (lower) for the BUF420 as a buck converter driven by a simple cascode

The results suggest that the cascode connection of a BJT can offer an improvement in switching speed and should be considered when designing SiC BJT drive circuits. Sample devices for the BitSiC1206 were prohibitively expensive, preventing the complete evaluation of their performance with a cascode drive.

5. SiC JFET in cascode drive

There are many examples of high voltage normally-on SiC JFETs being connected in cascode with a silicon MOSFET [80-86] or a low voltage normally-off SiC JFET [87], to achieve a normally-off compound switch. The popularity of the cascode has led to the development of a normally-on JFET that is co-packaged with a silicon MOSFET [87].

The normally-off JFETs developed by Semisouth do not suffer the problems of normally-on SiC JFETs, but require a sustained gate current. Rapid injection and removal of charge carriers remains essential to achieve fast switching with these devices.

Tests were conducted to evaluate whether or not a cascode drive circuit would offer any benefit when driving normally-off SiC JFETs. The gate impedances in the test circuits in Figure A-1 and Figure A-4 were adjusted to limit the SiC JFET's sustained gate current to an appropriate level. The JFETs were tested in a 60V to 30V buck converter and the rise and fall times of their drain-source voltage were measured. The results are summarized in Table A-2. A clear improvement was observed with the cascode driver compared to the half-bridge driver.

JFET driver topology	Rise time	Fall time
Half-bridge	52ns	62ns
Cascode	23ns	28ns

Table A-2: Comparison of voltage transition times for the normally-off SiC JFET in a 60V to 30V buck converter with cascode and half-bridge gate drive circuits.

The voltage slew rates for this test were calculated and are shown in Table A-3.

JFET driver topology	Turn-off slew rate (kV/µs)	Turn-on slew rate (kV/µs)
Half-bridge driver	1.15	0.97
Cascode	2.61	2.14

Table A-3:Comparison of slew rates for the normally-on SiC JFET in a 60V to 30V buck converter with cascode and half-bridge drivers

Although the normally-off SiC JFET achieves shorter switching times and higher slew rates with the cascode drive topology than the half-bridge driver, much larger slew rates were since observed in the PFC circuit in Chapter 6, where a two-stage drive circuit was used. Figure A-6 shows the normally-off SiC JFET turning off in this application with a slew rate of 6.7kV/µs.

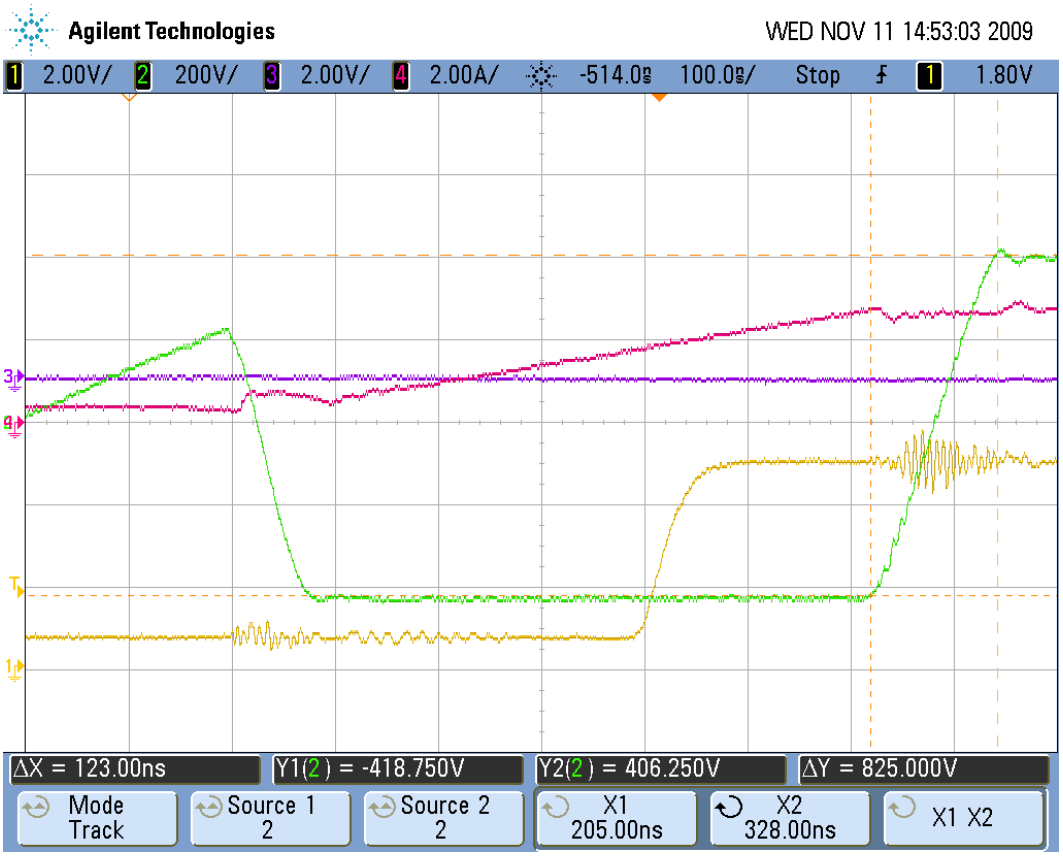
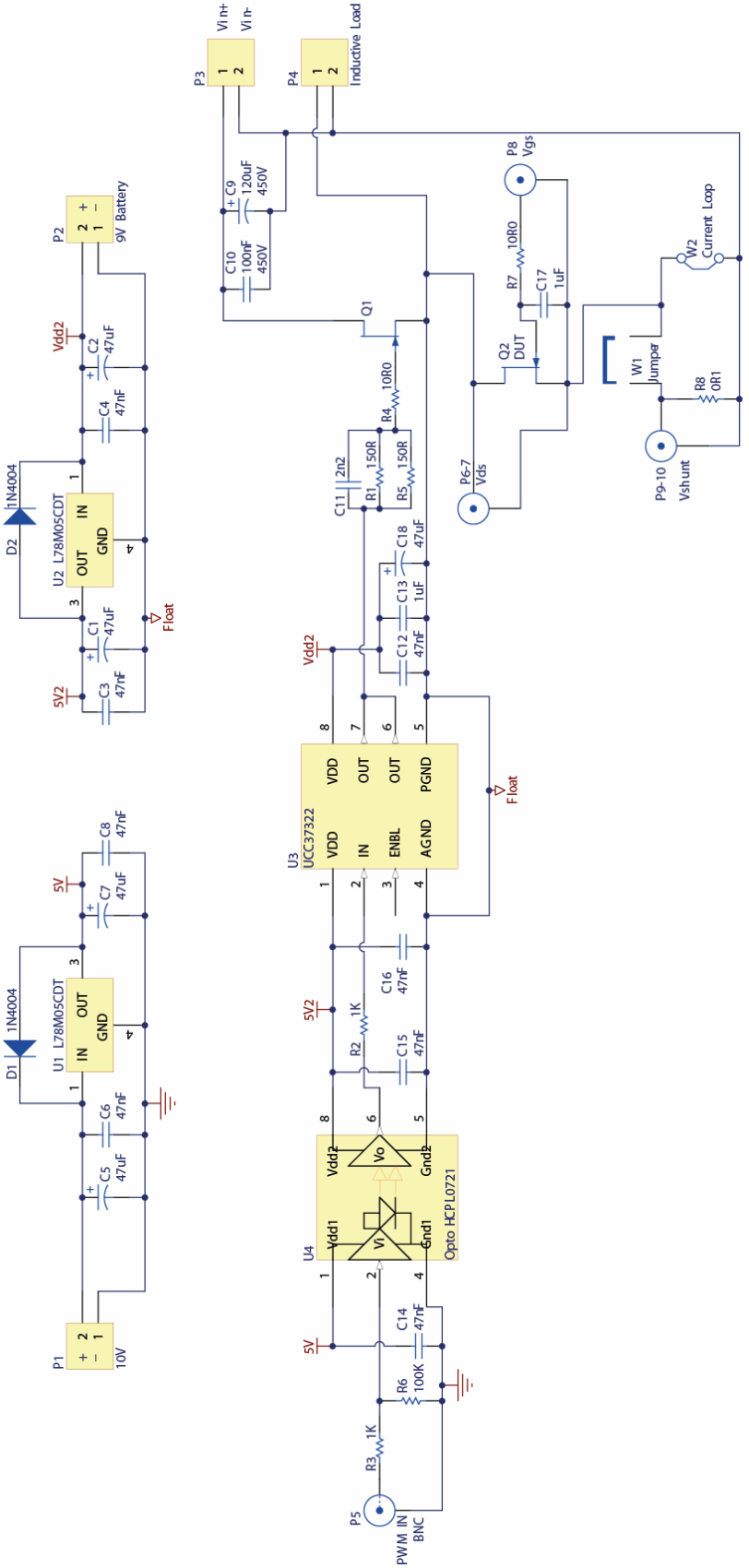


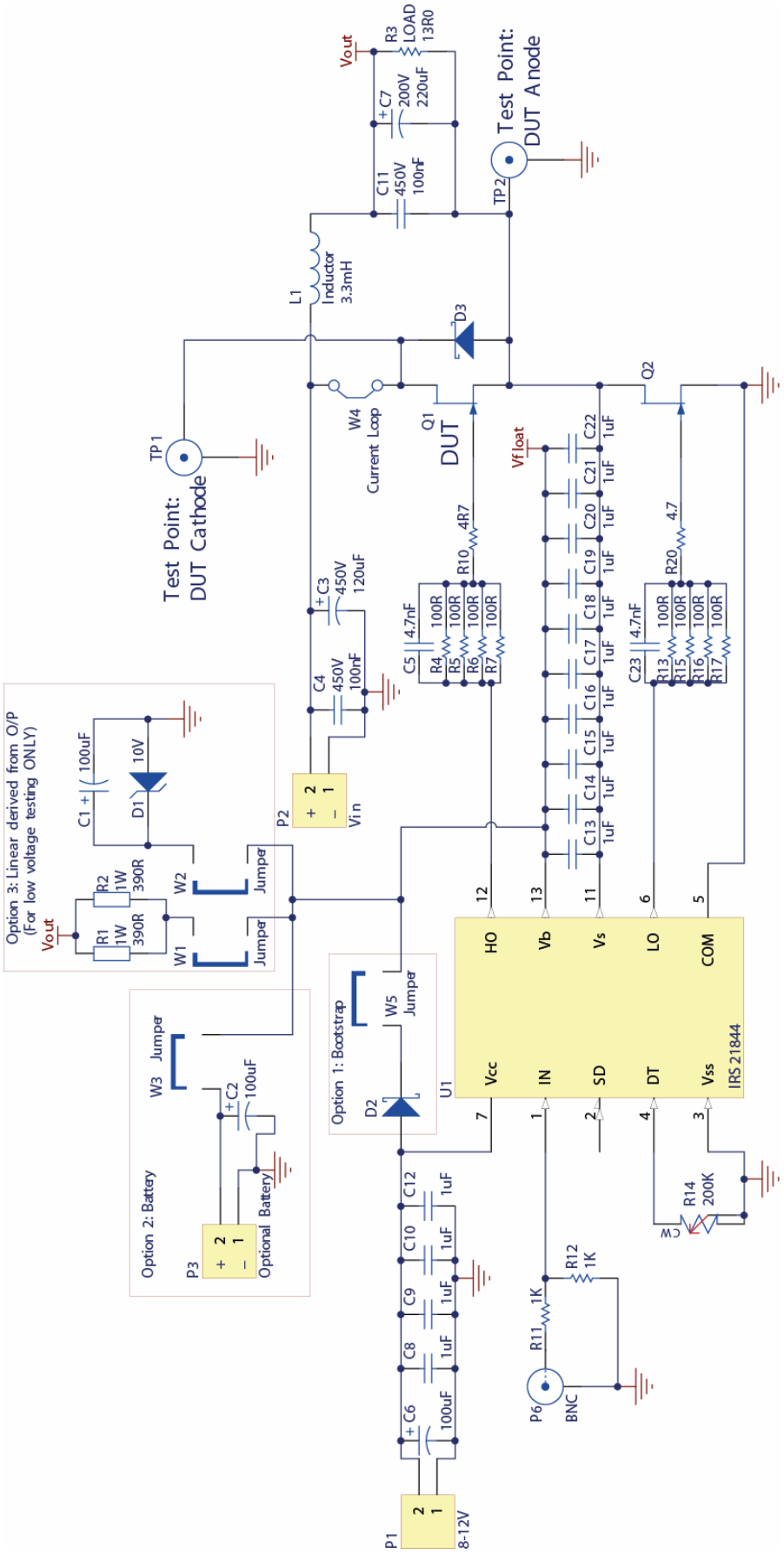
Figure A-6: The normally-off SiC JFET's drain-source voltage (green) in the PFC circuit rising 825V in 123ns during turn-off.

It is therefore recommended for future work that a direct comparison be made between the cascode drive circuit and the two-stage JFET drive circuit in a high voltage application to determine conclusively which topology allows the normally-off SiC JFET to achieve the highest switching speeds.

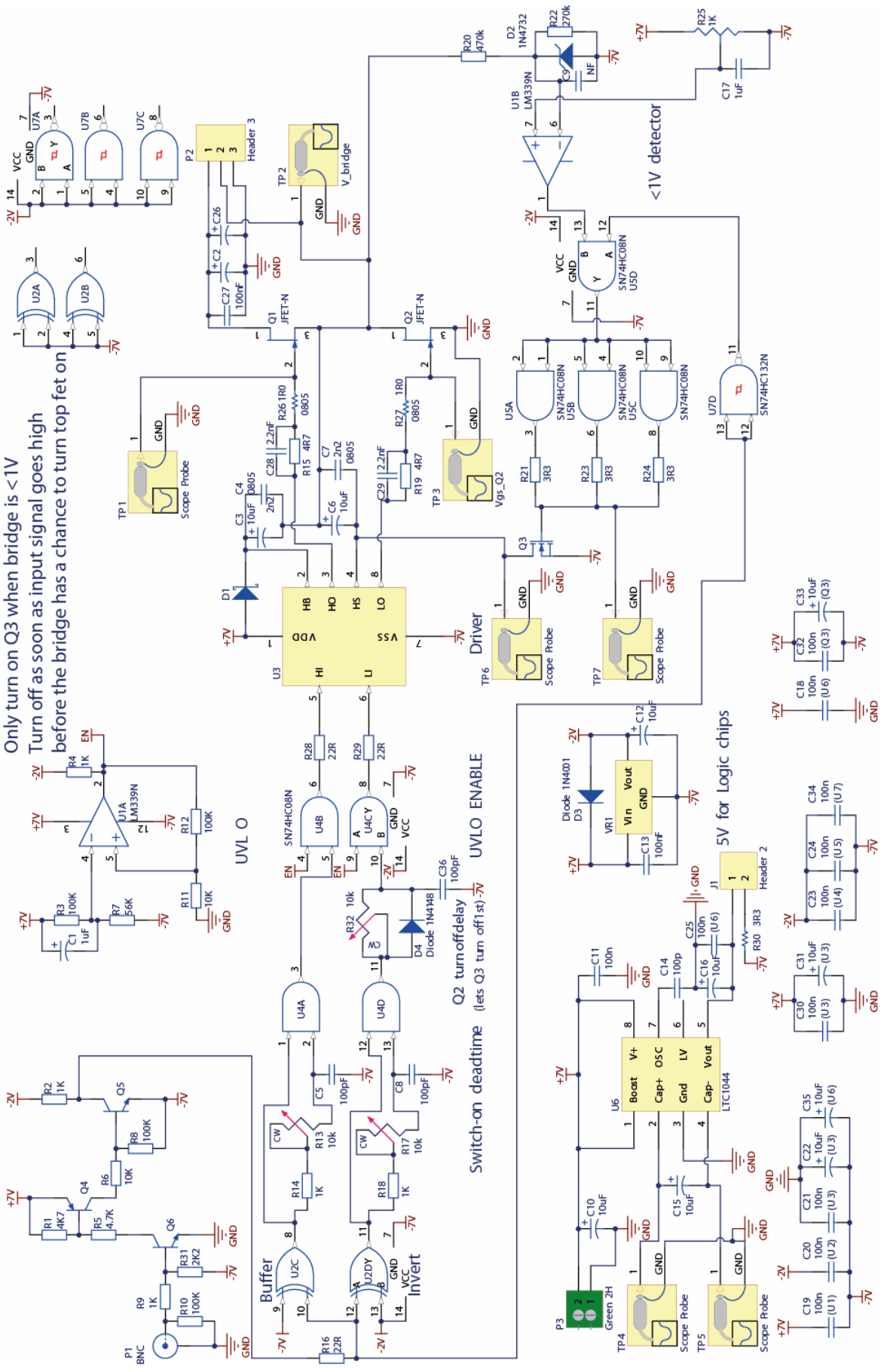
Appendix B. Complete Schematic Diagrams



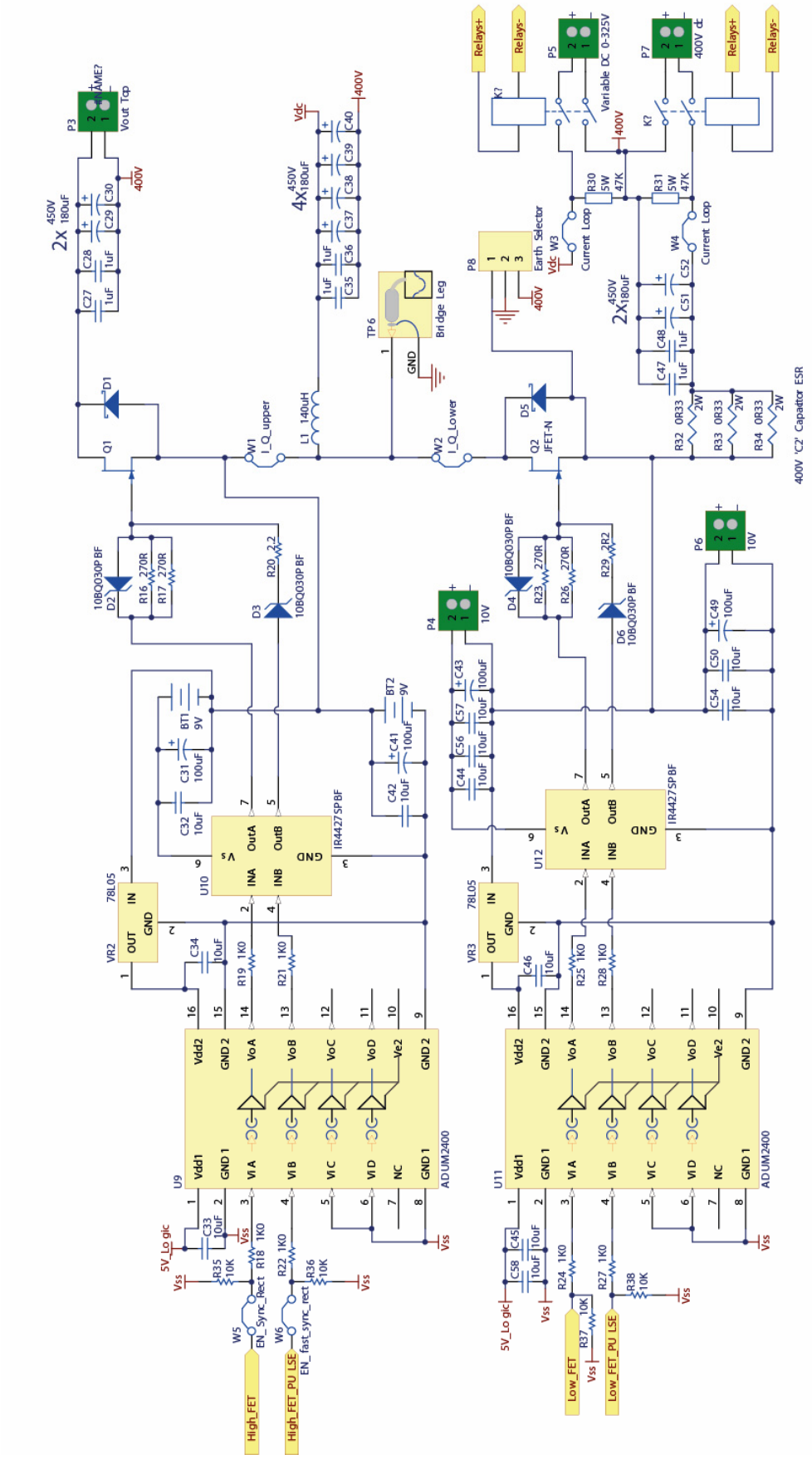
Schematic 1: Reverse recovery test circuit



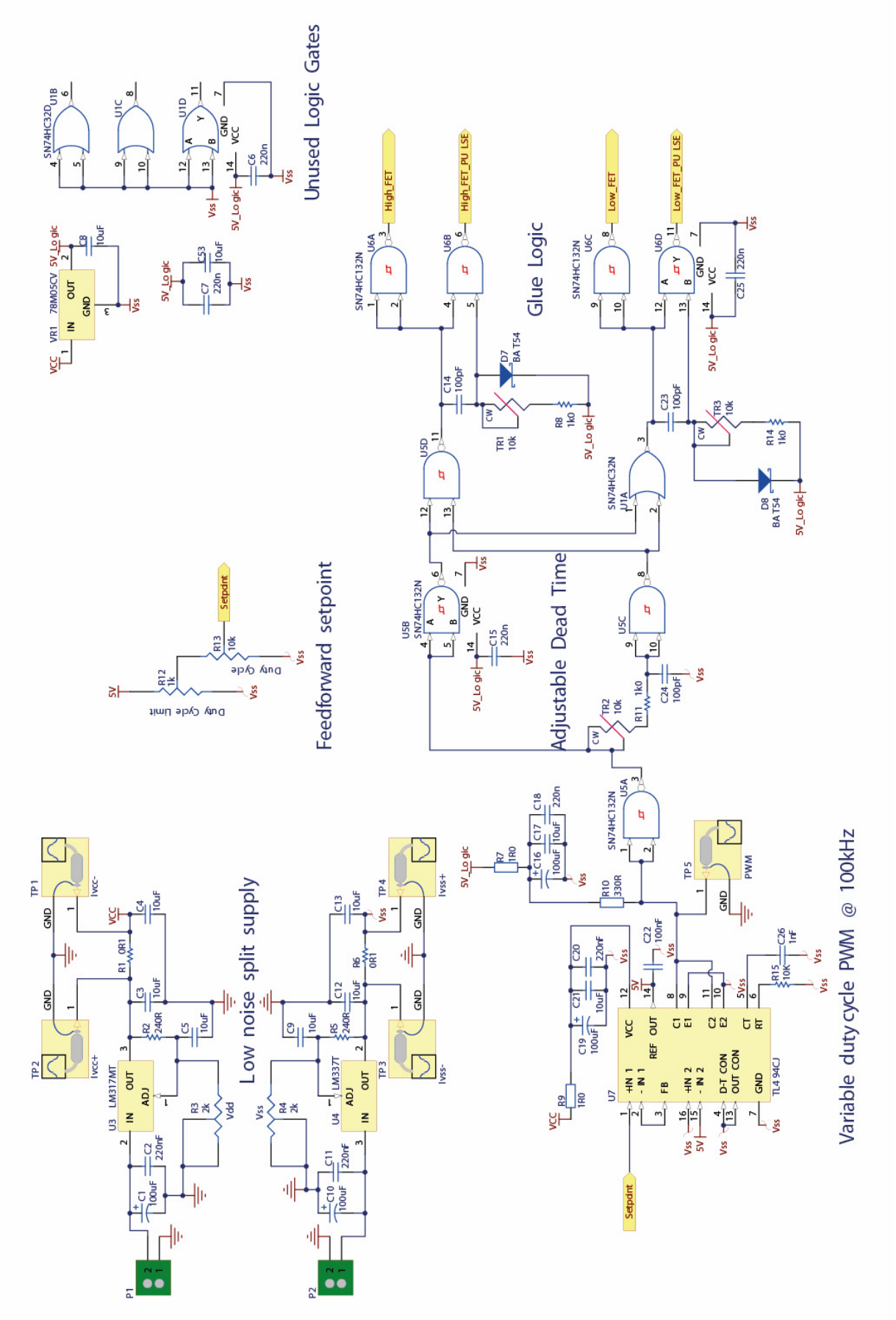
Schematic 2: Synchronous rectification test circuit



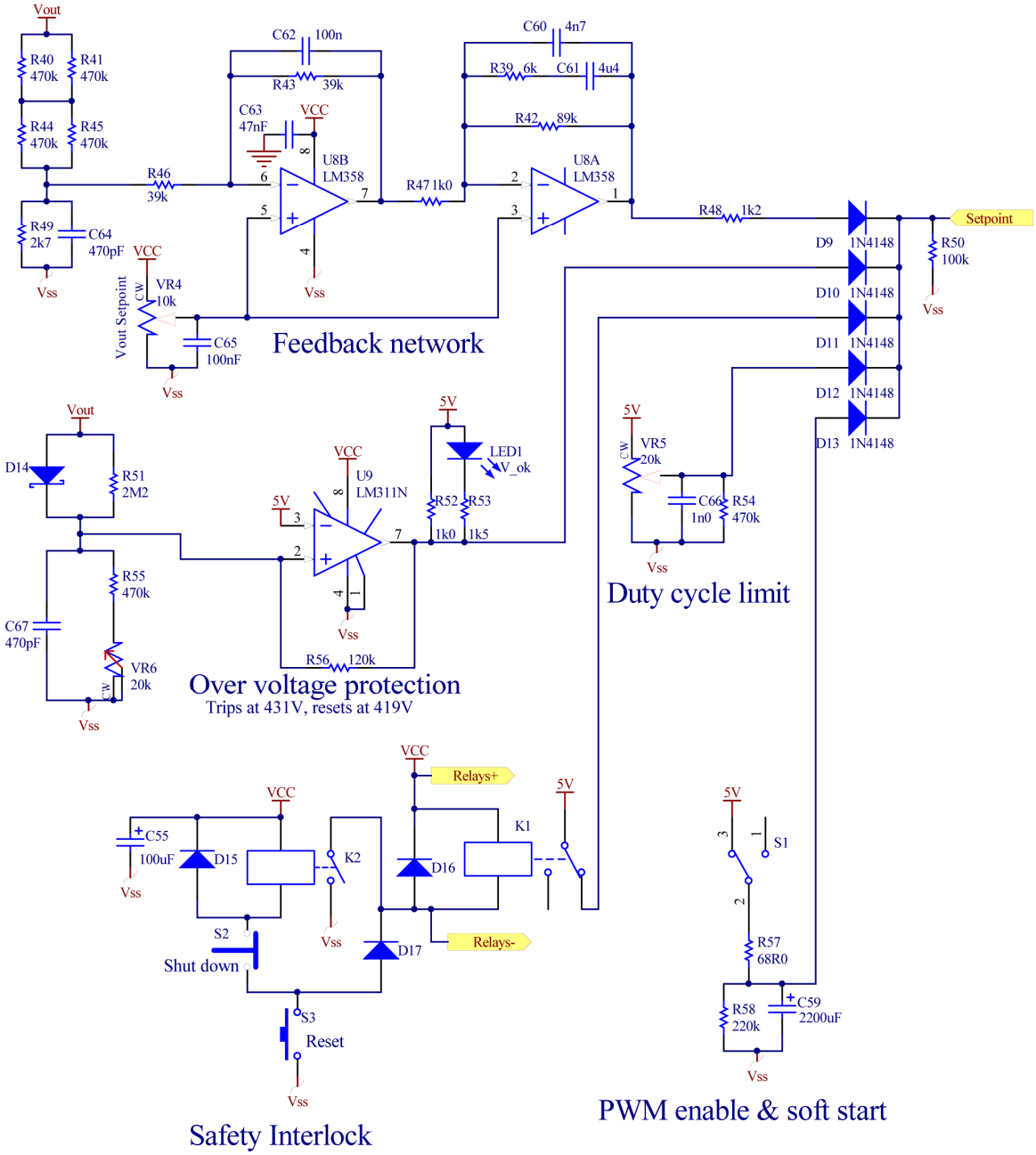
Schematic 3: SiC JFET driver circuit



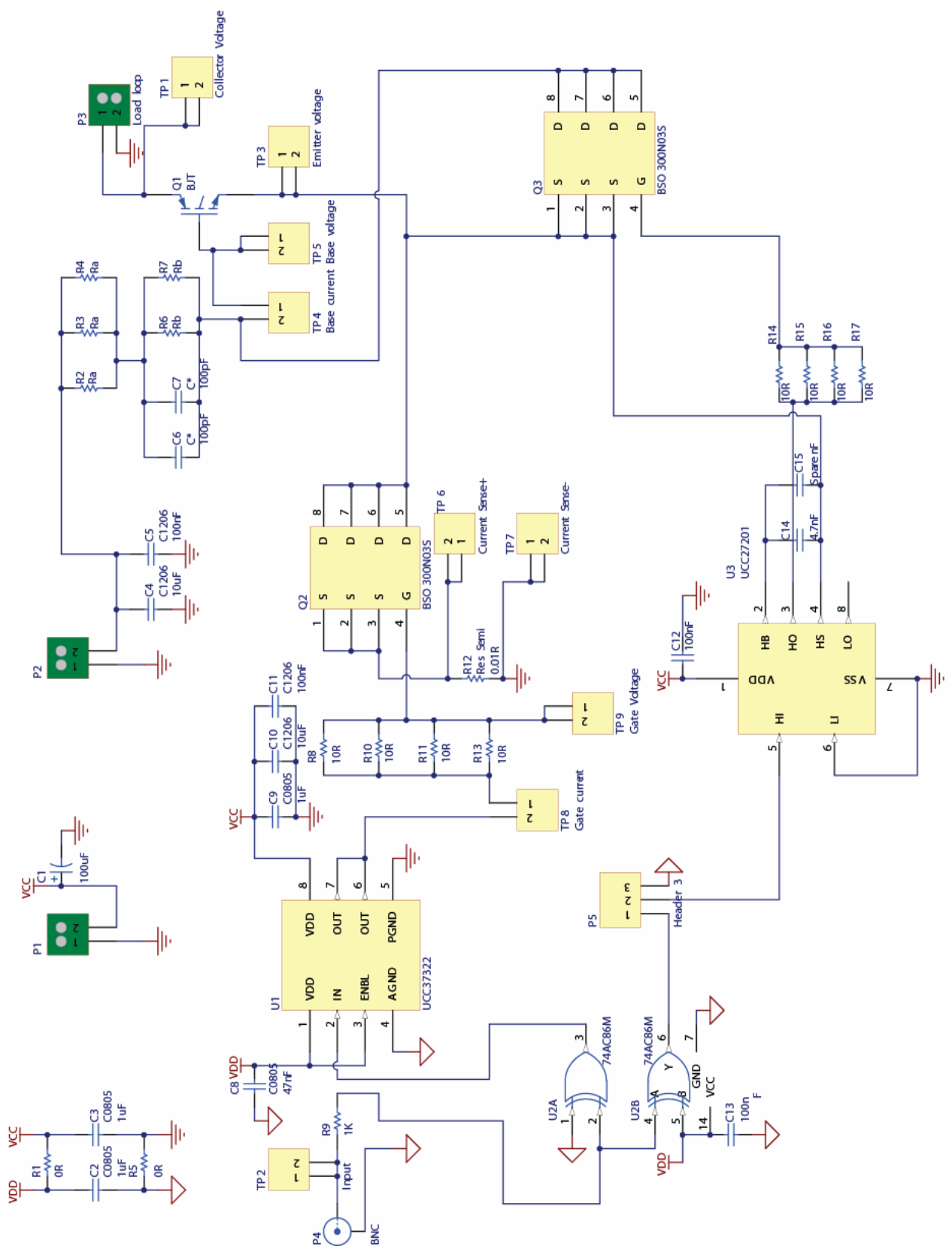
Schematic 4: PFC output circuit



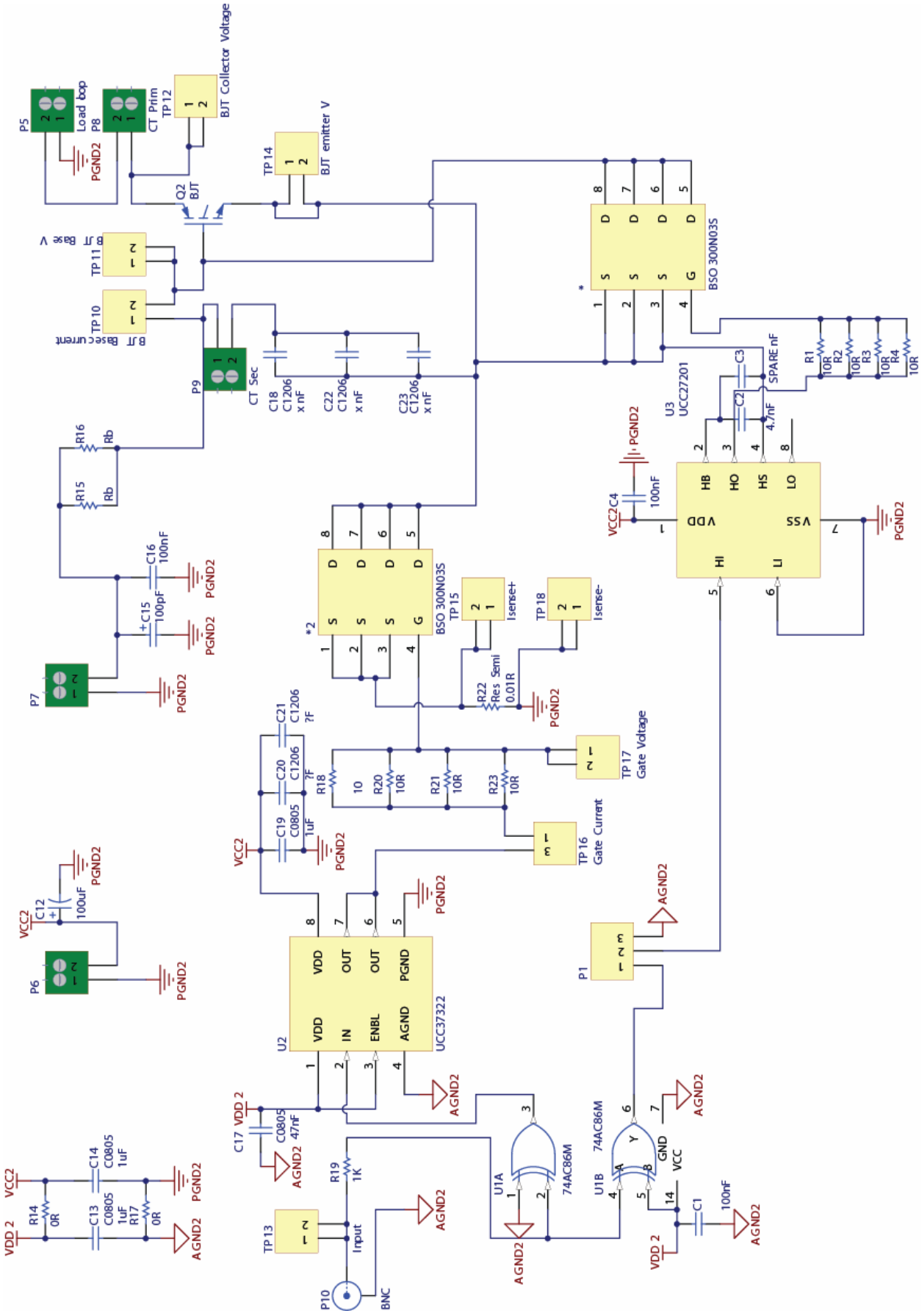
Schematic 5: PFC control circuit



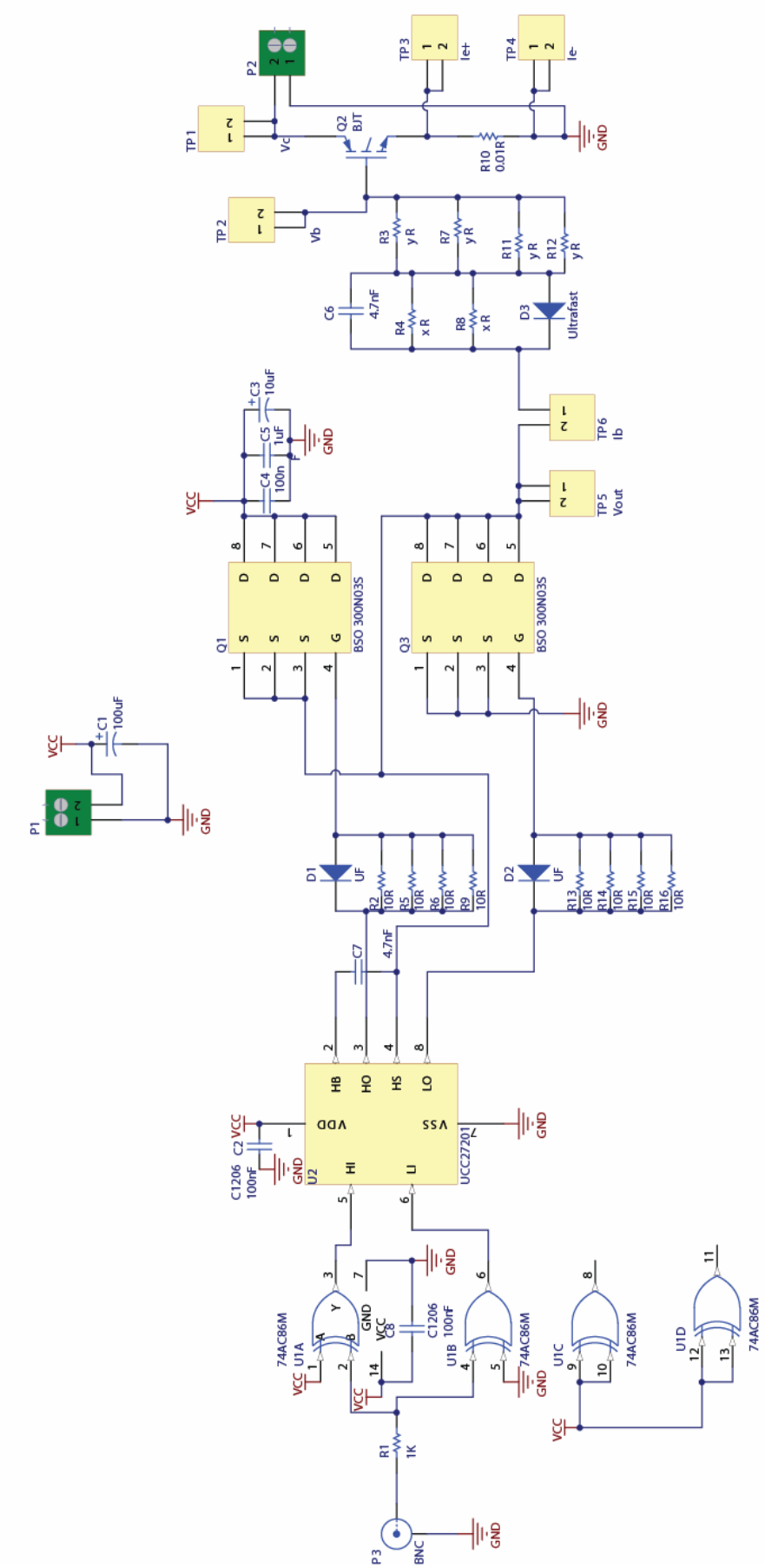
Schematic 6: PFC control circuit



Schematic 7: Cascode drive circuit



Schematic 8: Cascode drive circuit with proportional drive from current transformer



Schematic 9: Half-bridge BJT drive circuit for comparison to cascode

Appendix C. SJEP120R125 SiC JFET Datasheet

Excerpt reproduced from [11].

SemiSouth

PRELIMINARY

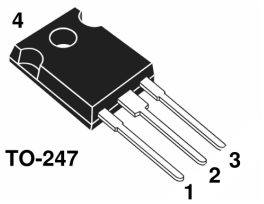
Silicon Carbide

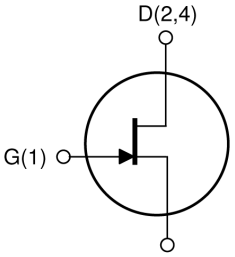
SJEP120R125

Normally-OFF Trench Silicon Carbide Power JFET

Product Summary		
BV_{DS}	1200	V
$R_{DS(ON)max}$	0.125	Ω
$E_{TS,typ}$	170	µJ

Features:
- Compatible with Standard Gate Driver ICs
- Positive Temperature Coefficient for Ease of Paralleling
- Temperature Independent Switching Behavior
- 175 ℃ Maximum Operating Temperature
- $R_{DS(on)max}$ of 0.125 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance





Internal Schematic

Applications:
- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	$I_{D,\ Tj=125}$	T_j = 125 ℃	15	A
	$I_{D,\ Tj=175}$	T_j = 175 ℃	10	
Pulsed Drain Current [1]	I_{DM}	T_C = 25 ℃	30	A
Short Circuit Withstand Time	t_{SC}	V_{DD} < 800 V, T_C < 125 ℃	50	µs
Power Dissipation	P_D	T_C = 25 ℃	136	W
Gate-Source Voltage	V_{GS}	static	-15 to +3	V
		AC[2]	-15 to +15	V
Operating and Storage Temperature	T_j, $T_{j,stg}$		-55 to +175	℃
Lead Temperature for Soldering	T_{sold}	1/8" from case < 10 s	260	℃

[1] Limited by pulse width
[2] Rg_{EXT} = 1 ohm, $t_o \leq$ 200ns

THERMAL CHARACTERISTICS

Parameter	Symbol	Value		Unit
		Typ	Max	
Thermal Resistance, junction-to-case	$R_{th,JC}$	-	1.1	℃ / W
Thermal Resistance, junction-to-ambient	$R_{th,JA}$	-	50	

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Off Characteristics						
Drain-Source Blocking Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 600 µA	1200	-	-	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, Tj = 25°C	-	100	600	µA
		V_{DS} = 1200 V, V_{GS} = 0 V, Tj = 175°C	-	300	-	
		V_{DS} = 1200 V, V_{GS} ≤ -15 V, Tj = 25°C	-	1	-	
		V_{DS} = 1200 V, V_{GS} ≤ -15 V, Tj = 175°C	-	10	-	
Total Gate Reverse Leakage	I_{GSS}	V_{GS} = -15 V, VDS = 0V	-	-0.1	-0.3	mA
		V_{GS} = -15 V, VDS = 1200V	-	-0.1	-	
On Characteristics						
Drain-Source On-resistance	$R_{DS(on)}$	I_D = 12 A, V_{GS} = 3 V, T_j = 25 °C	-	0.09	0.125	Ω
		I_D = 12 A, V_{GS} = 3 V, T_j = 125 °C	-	0.20	-	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 1 V, I_D = 34 mA	0.75	1.00	1.25	V
Gate Forward Current	I_{GFWD}	V_{GS} = 3 V	-	200	-	mA
Gate Resistance	R_G	f = 1 MHz, drain-source shorted	-	8	-	Ω
	$R_{G(ON)}$	V_{GS} >2.7V; See Figure 5	-	0.5	-	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DD} = 100 V	-	610	-	pF
Output Capacitance	C_{oss}		-	90	-	
Reverse Transfer Capacitance	C_{rss}		-	85	-	
Effective Output Capacitance, energy related	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	50	-	
Switching Characteristics						
Turn-on Delay	t_{on}	V_{DS} = 600 V, I_D = 12 A, Inductive Load, T_J = 25°C, Gate Driver = +15V, -10V, Rg_{EXT} = 5ohm, See Figure 15 and application note for gate drive recommendations	-	10	-	ns
Rise Time	t_r		-	12	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}		-	70	-	µJ
Turn-off Energy	E_{off}		-	100	-	
Total Switching Energy	E_{ts}		-	170	-	
Turn-on Delay	t_{on}	V_{DS} = 600 V, I_D = 12 A, Inductive Load, T_J = 150°C, Gate Driver = +15V, -10V, Rg_{EXT} = 5ohm, See Figure 15 and application note for gate drive recommendations	-	10	-	ns
Rise Time	t_r		-	15	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}		-	85	-	µJ
Turn-off Energy	E_{off}		-	100	-	
Total Switching Energy	E_{ts}		-	185	-	
Total Gate Charge	Q_g	V_{DS} = 600 V, I_D = 10 A, V_{GS} = + 2.5 V	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	24	-	

Figure 1. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 25 °C; parameter: V_{GS}

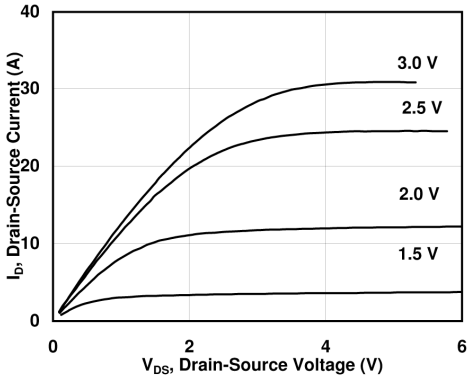


Figure 2. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 125 °C; parameter: V_{GS}

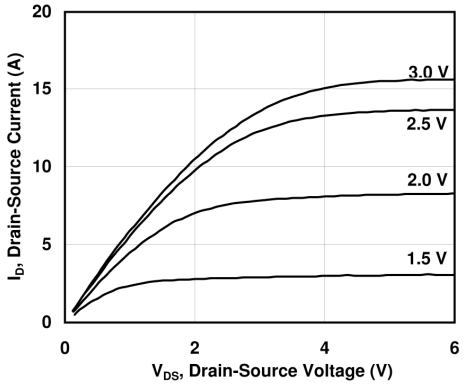


Figure 3. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 175 °C; parameter: V_{GS}

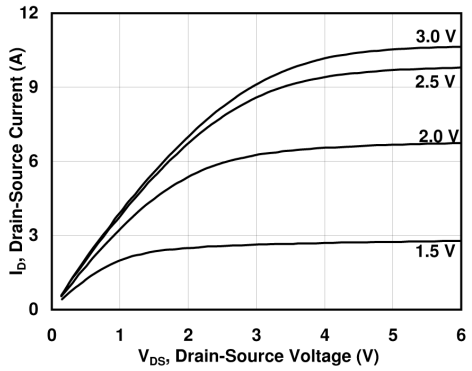


Figure 4. Typical Transfer Characteristics
$I_D = f(V_{GS})$; V_{DS} = 5 V

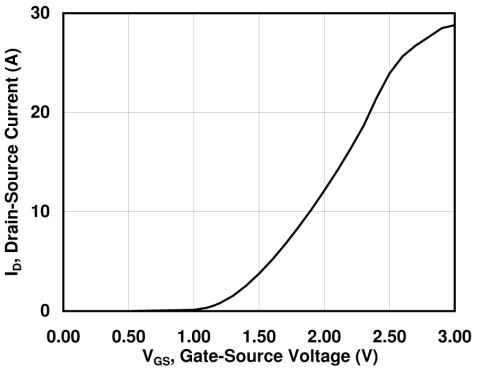


Figure 5. Gate-Source Current
$I_{GS} = f(V_{GS})$; parameter: T_j

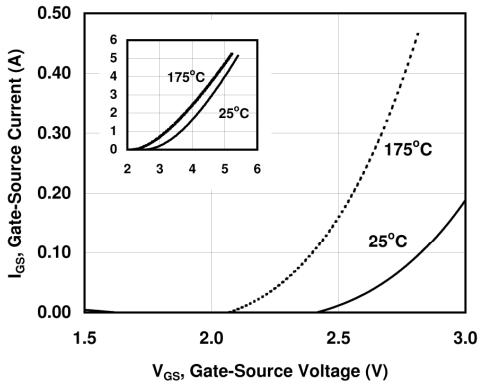


Figure 6. Drain-Source On-resistance
$R_{DS(on)} = f(I_D)$; V_{GS} = 3.0; parameter: Tj

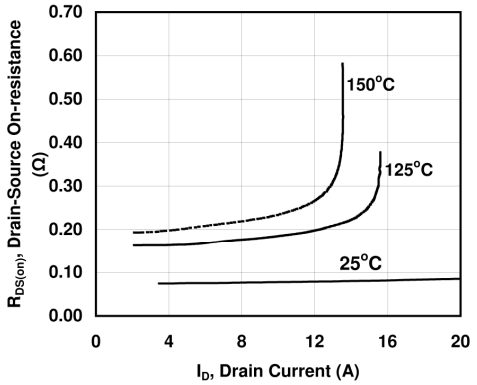


Figure 7. Drain-Source On-resistance

$R_{DS(ON)} = f(T_j)$; parameter: I_{GS}

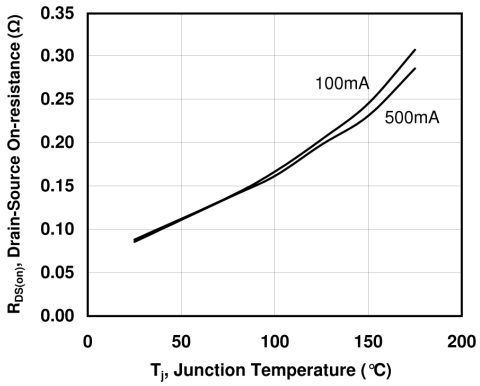


Figure 8. Drain-Source On-resistance

$R_{DS(ON)} = f(I_{GS})$; $T_j = 25^oC$

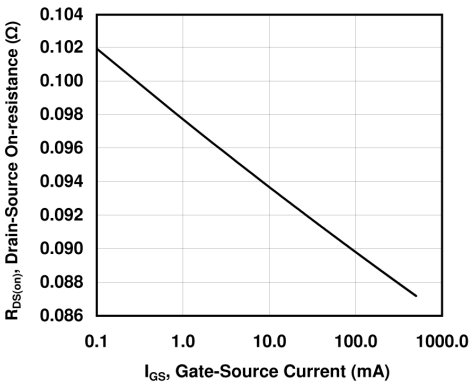


Figure 9. Typical Capacitance

$C = f(V_{DS})$; $V_{GS} = 0$ V; f = 1 MHz

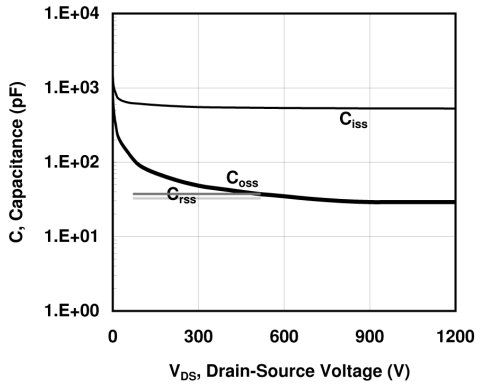


Figure 10. Gate Charge

$Q_g = f(V_{GS})$; $V_{DS} = 600V$; $I_D = 5A$, $T_j = 25^oC$

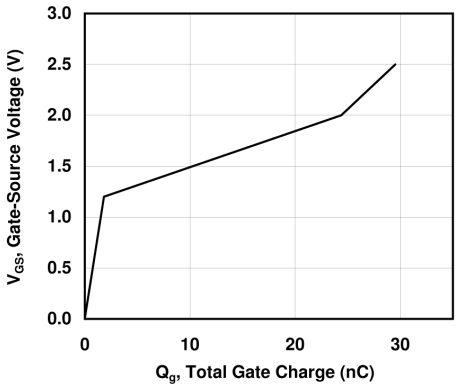


Figure 11. Gate Threshold Voltage

$V_{th} = f(T_j)$

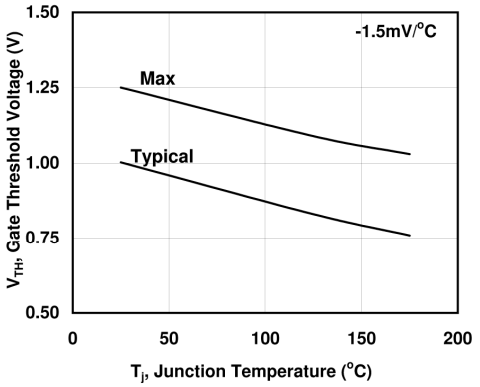


Figure 12. Drain-Source Leakage

$I_D = f(V_{DS})$; $V_{GS} = 0V$; parameter: Tj

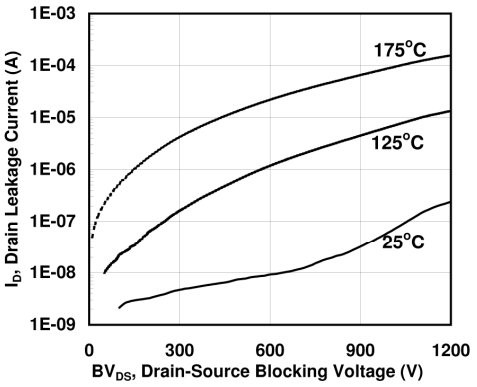


Figure 13. Switching Energy Losses
$E_s = f(I_D)$; V_{DS} = 600V; GD = +15V/-10V, R_{GEXT} = 5ohm

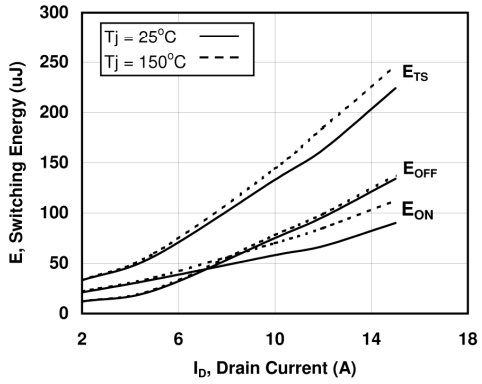


Figure 14. Switching Energy Losses
$E_s = f(R_{GEXT})$; V_{DS} = 600V; I_D = 12A, GD = +15V/-10V

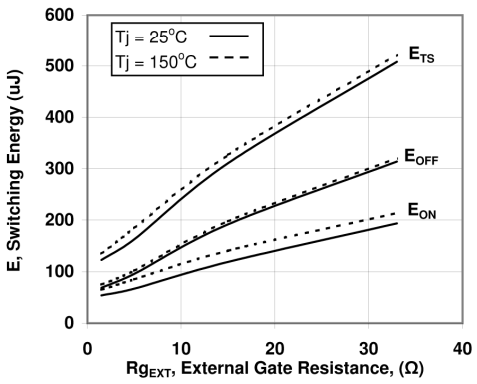


Figure 15. Inductive Load Switching Circuit

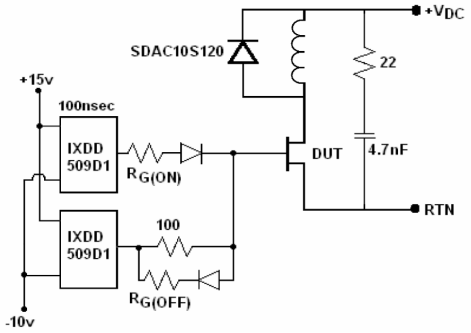
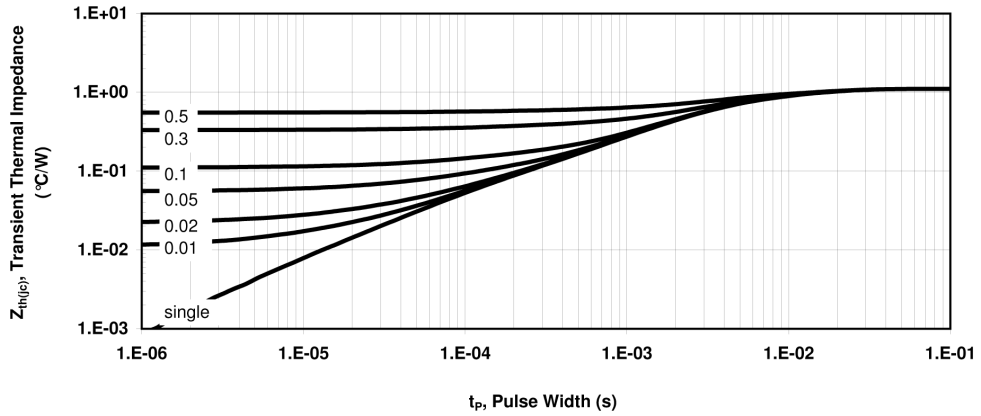


Figure 18. Transient Thermal Impedance
$Z_{th(jc)} = f(t_P)$; parameter: Duty Ratio



Appendix D. SJEP120R100 SiC JFET datasheet

Excerpt reproduced from [12].

SemiSouth

PRELIMINARY

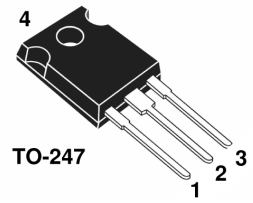
Silicon Carbide

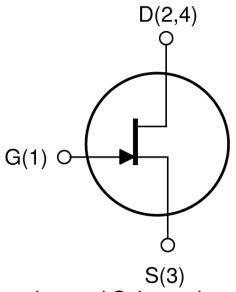
SJEP120R100

Normally-OFF Trench Silicon Carbide Power JFET

Product Summary		
BV_{DS}	1200	V
$R_{DS(ON)max}$	0.100	Ω
$E_{TS,typ}$	170	µJ

Features:
- Compatible with Standard Gate Driver ICs
- Positive Temperature Coefficient for Ease of Paralleling
- Extremely Fast Switching with No "Tail" Current at 150 ℃
- 175 ℃ Maximum Operating Temperature
- $R_{DS(on)max}$ of 0.100 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance





Internal Schematic

Applications:
- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	$I_{D,\ Tj=125}$	T_j = 125 ℃	17	A
	$I_{D,\ Tj=175}$	T_j = 175 ℃	12	
Pulsed Drain Current [1]	I_{DM}	T_C = 25 ℃	30	A
Short Circuit Withstand Time	t_{SC}	V_{DD} < 800 V, T_C < 125 ℃	50	µs
Power Dissipation	P_D	T_C = 25 ℃	136	W
Gate-Source Voltage	V_{GS}	AC[2]	-15 to +15	V
Operating and Storage Temperature	T_j, $T_{j,stg}$		-55 to +175	℃
Lead Temperature for Soldering	T_{sold}	1/8" from case < 10 s	260	℃

[1] Limited by pulse width
[2] Rg_{EXT} = 1 ohm, $t_p \leq$ 200ns, see Figure 5 for static conditions

THERMAL CHARACTERISTICS

Parameter	Symbol	Value		Unit
		Typ	Max	
Thermal Resistance, junction-to-case	$R_{th,JC}$	-	1.1	℃ / W
Thermal Resistance, junction-to-ambient	$R_{th,JA}$	-	50	

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Off Characteristics						
Drain-Source Blocking Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 600 µA	1200	-	-	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, Tj = 25°C	-	100	600	µA
		V_{DS} = 1200 V, V_{GS} = 0 V, Tj = 175°C	-	300	-	
		V_{DS} = 1200 V, V_{GS} ≤ -15 V, Tj = 25°C	-	1	-	
		V_{DS} = 1200 V, V_{GS} ≤ -15 V, Tj = 175°C	-	10	-	
Total Gate Reverse Leakage	I_{GSS}	V_{GS} = -15 V, VDS = 0V	-	-0.1	-0.3	mA
		V_{GS} = -15 V, VDS = 1200V	-	-0.1	-	
On Characteristics						
Drain-Source On-resistance	$R_{DS(on)}$	I_D = 12 A, V_{GS} = 3 V, T_j = 25 °C	-	0.08	0.1	Ω
		I_D = 12 A, V_{GS} = 3 V, T_j = 125 °C	-	0.20	-	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 1 V, I_D = 34 mA	0.75	1.00	1.25	V
Gate Forward Current	I_{GFWD}	V_{GS} = 3 V	-	220	-	mA
Gate Resistance	R_G	f = 1 MHz, drain-source shorted	-	8	-	Ω
	$R_{G(ON)}$	V_{GS} >2.7V; See Figure 5	-	0.5	-	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DD} = 100 V	-	670	-	pF
Output Capacitance	C_{oss}		-	103	-	
Reverse Transfer Capacitance	C_{rss}		-	97	-	
Effective Output Capacitance, energy related	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	60	-	
Switching Characteristics						
Turn-on Delay	t_{on}	V_{DS} = 600 V, I_D = 12 A, Inductive Load, T_J = 25°C, Gate Driver = +15V, -10V, Rg_{EXT} = 5ohm	-	10	-	ns
Rise Time	t_r		-	12	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}	See Figure 15 and application note for gate drive recommendations	-	70	-	µJ
Turn-off Energy	E_{off}		-	100	-	
Total Switching Energy	E_{ts}		-	170	-	
Turn-on Delay	t_{on}	V_{DS} = 600 V, I_D = 12 A, Inductive Load, T_J = 150°C, Gate Driver = +15V, -10V, Rg_{EXT} = 5ohm	-	10	-	ns
Rise Time	t_r		-	15	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}	See Figure 15 and application note for gate drive recommendations	-	85	-	µJ
Turn-off Energy	E_{off}		-	100	-	
Total Switching Energy	E_{ts}		-	185	-	
Total Gate Charge	Q_g	V_{DS} = 600 V, I_D = 10 A, V_{GS} = + 2.5 V	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	24	-	

Figure 1. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 25 °C; parameter: V_{GS}

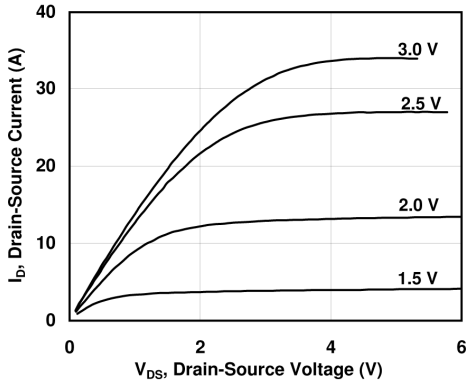

Figure 2. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 125 °C; parameter: V_{GS}

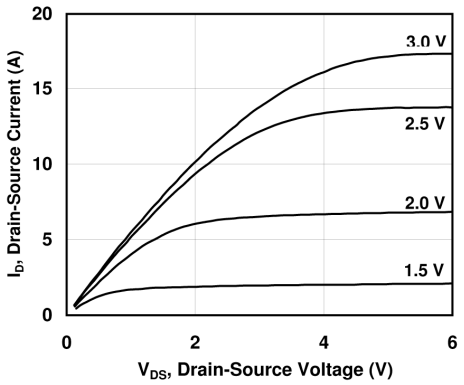

Figure 3. Typical Output Characteristics
$I_D = f(V_{DS})$; T_j = 175 °C; parameter: V_{GS}

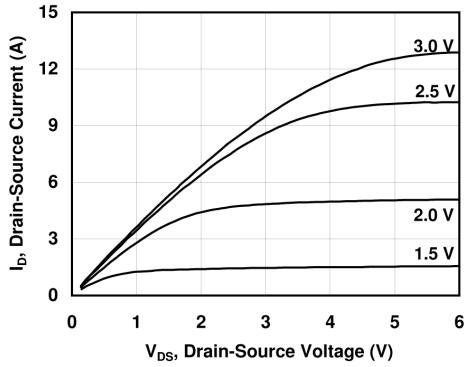

Figure 4. Typical Transfer Characteristics
$I_D = f(V_{GS})$; V_{DS} = 5 V

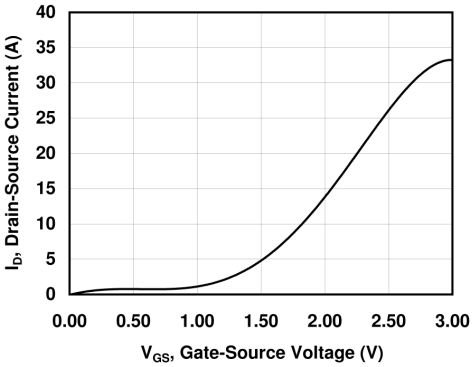

Figure 5. Gate-Source Current
$I_{GS} = f(V_{GS})$; parameter: T_j

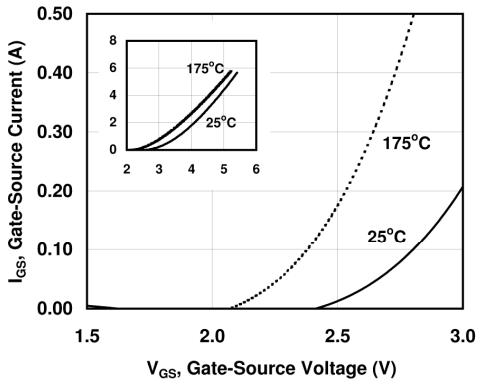

Figure 6. Drain-Source On-resistance
$R_{DS(on)} = f(I_D)$; V_{GS} = 3.0; parameter: Tj

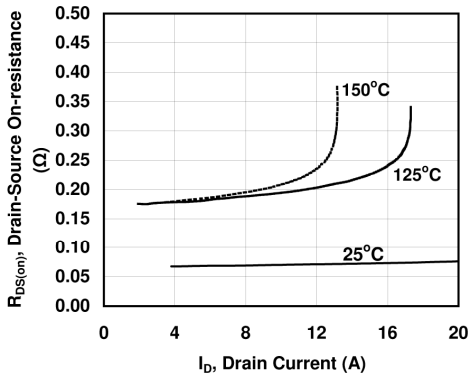

Figure 7. Drain-Source On-resistance

$R_{DS(ON)} = f(T_j)$; parameter: I_{GS}

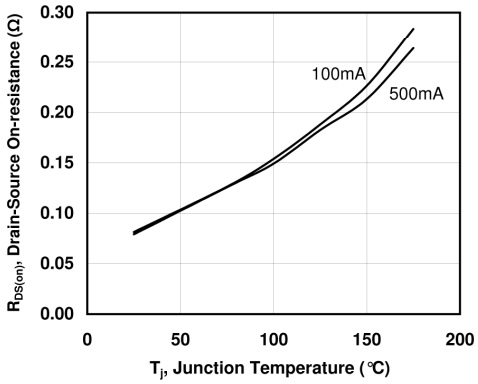

Figure 8. Drain-Source On-resistance

$R_{DS(ON)} = f(I_{GS})$; $T_j = 25^oC$

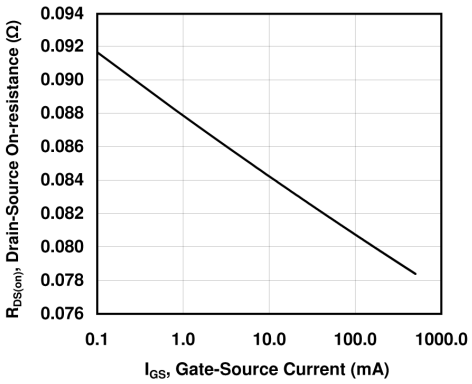

Figure 9. Typical Capacitance

$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

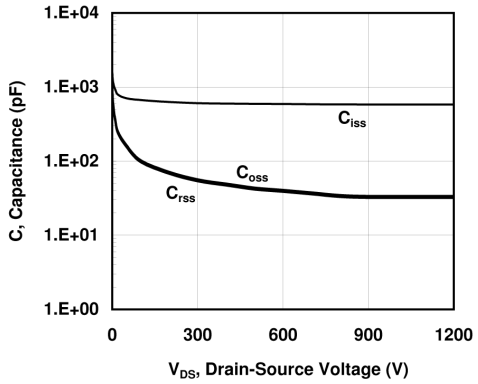

Figure 10. Gate Charge

$Q_g = f(V_{GS})$; V_{DS} = 600V; I_D = 5A, $T_j = 25^oC$

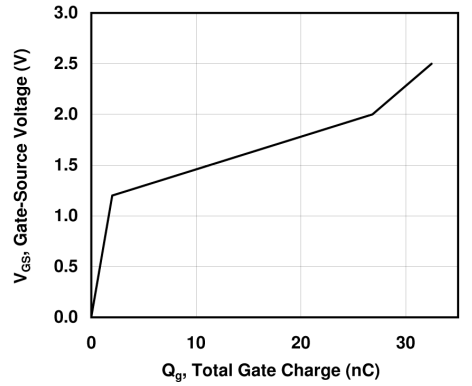

Figure 11. Gate Threshold Voltage

$V_{th} = f(T_j)$

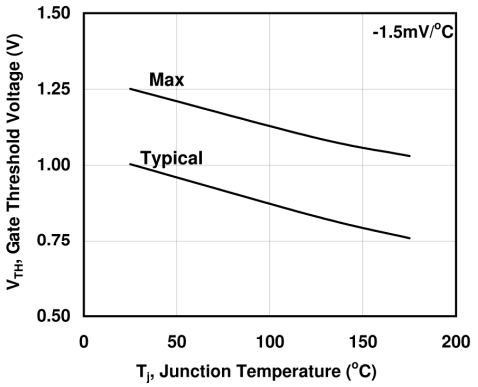

Figure 12. Drain-Source Leakage

$I_D = f(V_{DS})$; V_{GS} = 0V; parameter: Tj

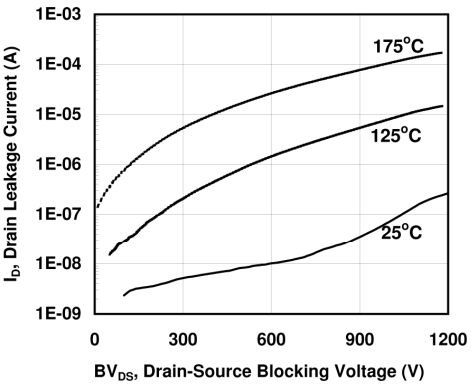

Figure 13. Switching Energy Losses
$E_s = f(I_D)$; V_{DS} = 600V; GD = +15V/-10V, R_{GEXT} = 5ohm

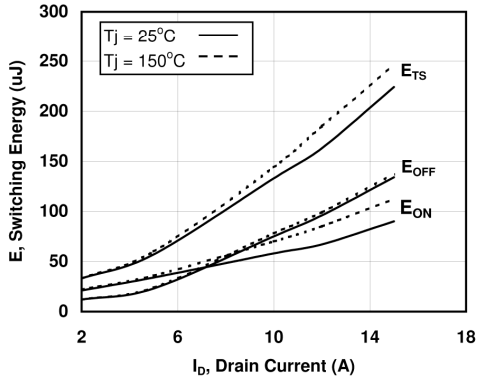

Figure 14. Switching Energy Losses
$E_s = f(R_{GEXT})$; V_{DS} = 600V; I_D = 12A, GD = +15V/-10V

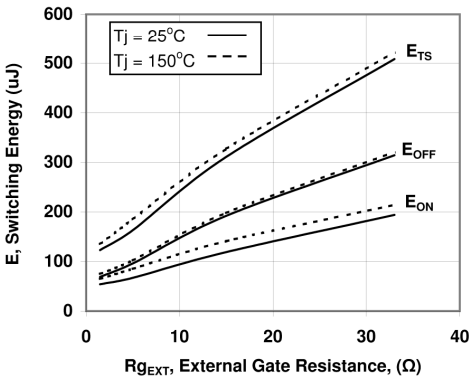

Figure 15. Inductive Load Switching Circuit

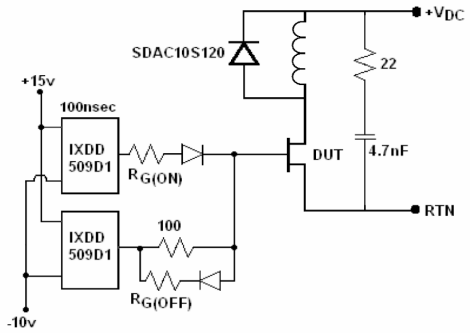

Figure 18. Transient Thermal Impedance
$Z_{th(jc)} = f(t_P)$; parameter: Duty Ratio